

Application Note

AN\_434\_FT602\_I2C\_User\_Guide

**Version** 0.1

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This application note describes how to use I2C master for sideband configuration from a user supplied host application.

The FT260 is a USB device which supports I²C and UART communication through the standard USB HID interface. This guide describes the FT260 HID report formats, and is intended for developers who are creating applications, extending FTDI provided applications or implementing FTDI’s applications for the FT260.

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# Introduction

The FT602 device uses the on-board I2C master interface exchange configuration information with the FIFO master. The FIFO master is required to implement a fixed set of I2C slave registers to receive information from the device during initialisation and also from the UVC host driver. The I2C interface may also be used for general purpose access to additional I2C slaves on the bus. This document shows how this may be achieved.

## Overview

The FT602 provides an I2C bus which operates as master with a default transmission speed of 1Mb/s. This speed is configurable and may be chosen from amongst 100Kb/s, 400Kb/s and 1Mb/s through the configuration programmer.

When using video capture applications, when any UVC control value is changed, a UVC control message is sent to the UVC device (FT602). The device, in turn, relays the message to the FPGA using the I2C Interface. The I2C slave address to be used for this communication is set via the configuration programmer. The I2C slave (e.g. FPGA or FIFO Master) shall implement the registers described in the next sections. Apart from these registers, I2C slave may implement custom registers which are controlled or configured through a user application.

# Auxiliary Interface

The FT602 UVC device supports up to 4 video channels and 1 auxiliary interface. All the I2C related commands from the user application are communicated over the auxiliary interface. Auxiliary interface isoptional and may be disabled when it is not required in the product application. When the interface is enabled, it isenumerated as highlighted in the below picture.

Section [3](#_Enable_/_Disable), describes the process for enabling / disabling the auxiliary interface.

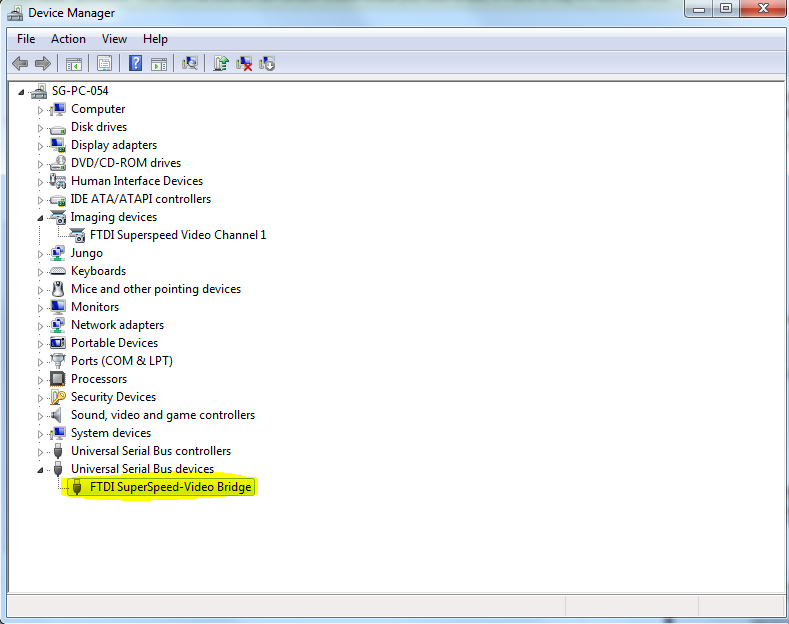


Figure 1 Auxiliary interface highlighted

The auxiliary interface uses Microsoft WinUSB drivers. In most cases, Windows is able to successfully install WinUSB drivers automatically from Windows Update. However, on certain versions WinUSB drivers for this interface may not load or install successfully. In such cases, manual installation of WinUSB drivers is required.

For manual installation follow the below steps:

1. Double click FT602WinUSBInstallation.exe.
2. Click on the ‘extract’ button to unpack the installer.



Figure 2 WinUSB Setup Procedure

1. Click Next.

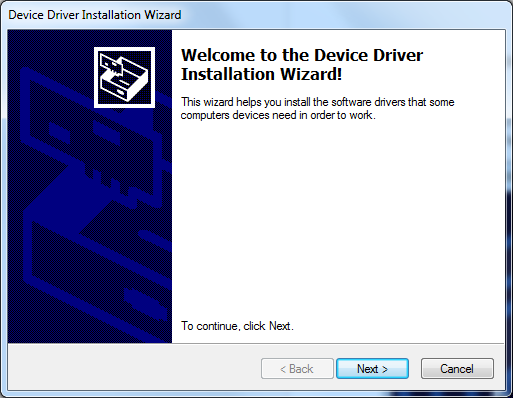


Figure 3 WinUSB Setup Procedure

1. Select ‘I accept this agreement’ and click Next.

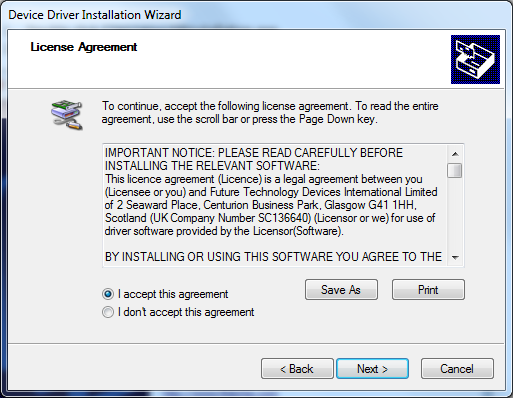


Figure 4 WinUSB Setup Procedure

1. Click on Finish button. Installation is completed.

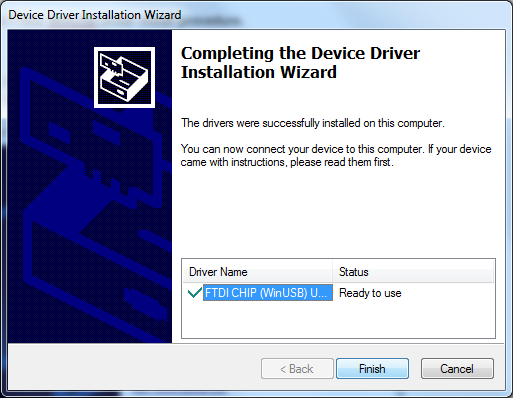


Figure 5 WinUSB Setup Procedure

# Enable / Disable Auxiliary Interface.

To enable/disable the auxiliary interface, launch the FT602 Configuration Programmer. Check the option “Auxiliary Interface” and then click “Write Configuration” to enable the interface. Uncheck the option and write configuration to disable the interface.

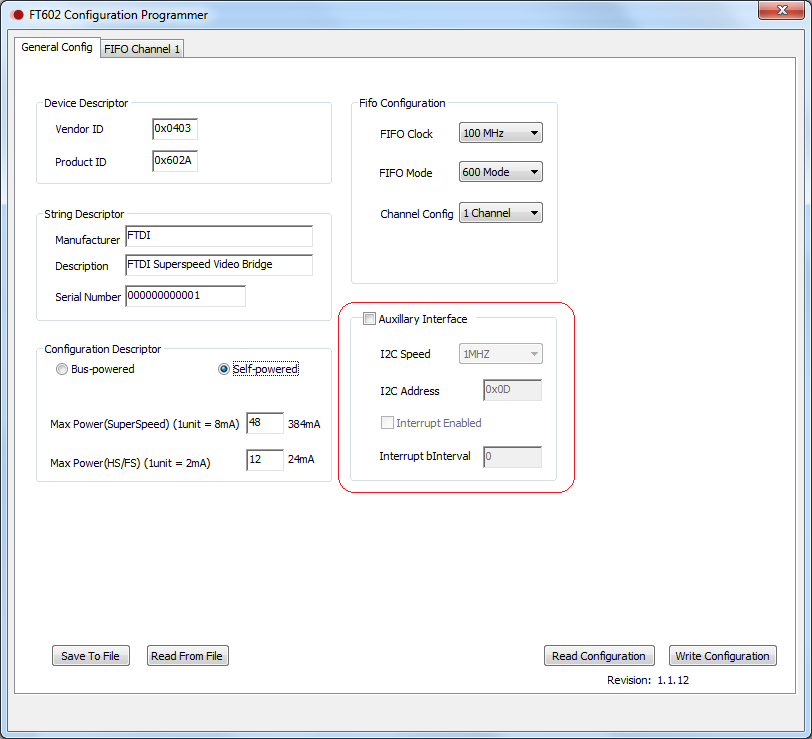


Figure 6 Enable / Disable Auxiliary Interface

# I2C Register Description

1. The I2C registers have different widths and must be written or read in full.
2. In the following, some registers use a unit of pixel clock. The pixel clock depends on the frame resolution and the selected frame rates. Table 3 – Pixel Clockprovides the frame resolutions and pixel clock frequency
3. 16 bytes of software defined registers are provided (e.g. scratch) per channel for storing UVC control and command information for storage and retrieval. Customer designs may act on the values written into these locations or provide a response to the USB host via these locations. The IRQ signal may be used to signal the host of change in conditions in the FPGA.

* **Convention**

RO: Read Only

RW: Read, Write

Device Address: 0x0D (seven bits address)

| **Address** | **Name** | **Size**  **(Byte)** | **Type** | **Description** | **Default** |
| --- | --- | --- | --- | --- | --- |
| 0x00 | Configuration | 1 | RW | bit[7:4]: reserved  bit[3]: I2C interrupt, 0 = disable, 1 = enable  bit[2:1]:  2’b00 = unknown speed  2’b01 = Super Speed  2’b10 = High Speed  2’b11 = Full Speed  B[0]: FIFO Mode, 0 = FT245, 1 = FT600 | 0x03 |
| 0x01 | FT602  Power Status | 1 | RW | Bit[7:2]: Reserved  Bit[1:0]: FT602 Power Status  00: Active  01: Suspend  1x: Power off | 0x00 |
| 0x10 | Ch0\_Control | 2 | RW | Bit[15:8]:Frame Rate  00-01: 1 Frame per second  02-0xFF: 2-255 frames per second  Bit[7]: Pattern Select  0: Moving Pattern  1: Fixed Pattern  Bit[6:5]: Four kind of patterns  2’b11: 3 vertical bars  2’b10: 5 vertical bars  2’b01: 7 vertical bars  2’b00: 8 vertical bars  Bit[4:0]: Reserved | 0x3C00 |
| 0x11 | Ch0\_LSG\_LEG | 2 | RW | Bit[15:8]: Line Start Gap (units of pixel clock)  Bit[7:0]: Line End Gap (units of pixel clock) | 0x0804 |
| 0x12 | Ch0\_DSG\_DEG | 2 | RW | Bit[15:8]: Data Start Gap (units of pixel clock)  Bit[7:0]: Data End Gap (units of pixel clock) | 0x0804 |
| 0x13 | Ch0\_H\_Blank | 2 | RW | Number of clock cycle of H Blank (units of pixel clock) | 0x0010 |
| 0x14 | Ch1\_Control | 2 | RW | Bit[15:8]:Frame Rate  00-01: 1 frame per second  02-0xFF: 2-255 frames per second  Bit[7]: Pattern Select  0: Moving Pattern  1: Fixed Pattern  Bit[6:5]: Four kind of patterns  2’b11: 3 vertical bars  2’b10: 5 vertical bars  2’b01: 7 vertical bars  2’b00: 8 vertical bars  Bit[4:0]: Reserved | 0x3C20 |
| 0x15 | Ch1\_LSG\_LEG | 2 | RW | Bit[15:8]: Line Start Gap (units of pixel clock)  Bit[7:0]: Line End Gap (units of pixel clock) | 0x0804 |
| 0x16 | Ch1\_DSG\_DEG | 2 | RW | Bit[15:8]: Data Start Gap (units of pixel clock)  Bit[7:0]: Data End Gap (units of pixel clock) | 0x0804 |
| 0x17 | Ch1\_H\_Blank | 2 | RW | Number of clock cycle of H Blank (units of pixel clock) | 0x0010 |
| 0x18 | Ch2\_Control | 2 | RW | Bit[15:8]:Frame Rate  00-01: 1 frame per second  02-0xFF: 2-255 frames per second  Bit[7]: Pattern Select  0: Moving Pattern  1: Fixed Pattern  Bit[6:5]: Four kind of patterns  2’b11: 3 vertical bars  2’b10: 5 vertical bars  2’b01: 7 vertical bars  2’b00: 8 vertical bars  Bit[4:0]: Reserved | 0x3C40 |
| 0x19 | Ch2\_LSG\_LEG | 2 | RW | Bit[15:8]: Line Start Gap (units of pixel clock)  Bit[7:0]: Line End Gap (units of pixel clock) | 0x0804 |
| 0x1A | Ch2\_DSG\_DEG | 2 | RW | Bit[15:8]: Data Start Gap (units of pixel clock)  Bit[7:0]: Data End Gap (units of pixel clock) | 0x0804 |
| 0x1B | Ch2\_H\_Blank | 2 | RW | Number of clock cycle of H Blank (units of pixel clock) | 0x0010 |
| 0x1C | Ch3\_Control | 2 | RW | Bit[15:8]:Frame Rate  00-01: 1 frame per second  02-0xFF: 2-255 frames per second  Bit[7]: Pattern Select  0: Moving Pattern  1: Fixed Pattern  Bit[6:5]: Four kind of patterns  2’b11: 3 vertical bars  2’b10: 5 vertical bars  2’b01: 7 vertical bars  2’b00: 8 vertical bars  Bit[4:0]: Reserved | 0x3C50 |
| 0x1D | Ch3\_LSG\_LEG | 2 | RW | Bit[15:8]: Line Start Gap (units of pixel clock)  Bit[7:0]: Line End Gap (units of pixel clock) | 0x0804 |
| 0x1E | Ch3\_DSG\_DEG | 2 | RW | Bit[15:8]: Data Start Gap (units of pixel clock)  Bit[7:0]: Data End Gap (units of pixel clock) | 0x0804 |
| 0x1F | Ch3\_H\_Blank | 2 | RW | Number of clock cycle of H Blank (units of pixel clock) | 0x0010 |
| 0x20 | Ch0\_Low\_Mark | 2 | RW | Water Mark of channel 0 | 0x0000 |
| 0x21 | Ch0\_High\_Mark | 2 | RW | Buffer size of channel 0 | 0x0FFF |
| 0x22 | Ch1\_Low\_Mark | 2 | RW | Water Mark of channel 1 | 0x0000 |
| 0x23 | Ch1\_High\_Mark | 2 | RW | Buffer size of channel 1 | 0x0FFF |
| 0x24 | Ch2\_Low\_Mark | 2 | RW | Water Mark of channel 2 | 0x0000 |
| 0x25 | Ch2\_High\_Mark | 2 | RW | Buffer size of channel 2 | 0x0FFF |
| 0x26 | Ch3\_Low\_Mark | 2 | RW | Water Mark of channel 3 | 0x0000 |
| 0x27 | Ch3\_High\_Mark | 2 | RW | Buffer size of channel 3 | 0x0FFF |
| 0x28 | Ch0\_Frame\_Drop | 4 | RW | Number of discarded frames of channel 0 | 0x0000\_0000 |
| 0x29 | Ch1\_Frame\_Drop | 4 | RW | Number of discarded frames of channel 1 | 0x0000\_0000 |
| 0x2A | Ch2\_Frame\_Drop | 4 | RW | Number of discarded frames of channel 2 | 0x0000\_0000 |
| 0x2B | Ch3\_Frame\_Drop | 4 | RW | Number of discarded frames of channel 3 | 0x0000\_0000 |
| 0x40-  0x5F | UVC Control Channel 0 | 16 | RW | Software Define | X |
| 0x60 | Ch0\_Start\_Stream | 9 | RW | Big Endian  Byte 0-1: Video Frame Width  Byte 2-3: Video Frame Height  Byte 4-7: Clock Frequency (specified in Hz)  Byte 8: Resolution index (defined in USB descriptor).  0 : VGA  1 : HD  2 : FHD  Others : unused | Byte 0-1: 0x0280 (640)  Byte 2-3: 0x01E0 (480)  Bytes 4-7:  0x019BFCC0 (27MHz)  Byte sequence (0-8):  {0x80, 0x02, 0xE0, 0x01,  0x01, 0x9B, 0xFC, 0xC0,  0x00} |
| 0x70-  0x8F | UVC Control Channel 1 | 16 | RW | Software Define | X |
| 0x90 | Ch1\_Start\_Stream | 9 | RW | Big Endian  Byte 0-1: Video Frame Width  Byte 2-3: Video Frame Height  Byte 4-7: Clock Frequency (specified in Hz)  Byte 8: Resolution index (defined in USB descriptor).  0 : VGA  1 : HD  2 : FHD  Others : unused | Byte 0-1: 0x0280 (640)  Byte 2-3: 0x01E0 (480)  Bytes 4-7:  0x019BFCC0 (27MHz)  Byte sequence (0-8):  {0x80, 0x02, 0xE0, 0x01,  0x01, 0x9B, 0xFC, 0xC0,  0x00} |
| 0xA0-  0xBF | UVC Control Channel 2 | 16 | RW | Software Define | X |
| 0xC0 | Ch2\_Start\_Stream | 9 | RW | Big Endian  Byte 0-1: Video Frame Width  Byte 2-3: Video Frame Height  Byte 4-7: Clock Frequency (specified in Hz)  Byte 8: Resolution index (defined in USB descriptor).  0 : VGA  1 : HD  2 : FHD  Others : unused | Byte 0-1: 0x0280 (640)  Byte 2-3: 0x01E0 (480)  Bytes 4-7:  0x019BFCC0 (27MHz)  Byte sequence (0-8):  {0x80, 0x02, 0xE0, 0x01,  0x01, 0x9B, 0xFC, 0xC0,  0x00} |
| 0xD0-  0xEF | UVC Control Channel 3 | 16 | RW | Software Define | X |
| 0xF0 | Ch3\_Start\_Stream | 9 | RW | Big Endian  Byte 0-1: Video Frame Width  Byte 2-3: Video Frame Height  Byte 4-7: Clock Frequency (specified in Hz)  Byte 8: Resolution index (defined in USB descriptor).  0 : VGA  1 : HD  2 : FHD  Others : unused | Byte 0-1: 0x0280 (640)  Byte 2-3: 0x01E0 (480)  Bytes 4-7:  0x019BFCC0 (27MHz)  Byte sequence (0-8):  {0x80, 0x02, 0xE0, 0x01,  0x01, 0x9B, 0xFC, 0xC0,  0x00} |

Table 1 - I2C Registers

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| UVC Control Register Address | | | | Register Name | Description |
| Channel 1 | Channel 2 | Channel 3 | Channel 4 |  |  |
| 40 | 70 | A0 | D0 | REG\_CT\_AE\_MODE | Auto Exposure Mode |
| 41 | 71 | A1 | D1 | REG\_CT\_AE\_PRIORITY | Auto Exposure Priority |
| 42 | 72 | A2 | D2 | REG\_CT\_EXPOSURE\_TIME\_ABSOLUTE | Exposure Time Absolute |
| 43 | 73 | A3 | D3 | REG\_CT\_EXPOSURE\_TIME\_RELATIVE | Exposure Time Relative |
| 44 | 74 | A4 | D4 | REG\_CT\_FOCUS\_ABSOLUTE | Focus Absolute |
| 45 | 75 | A5 | D5 | REG\_CT\_FOCUS\_RELATIVE | Focus Relative |
| 46 | 76 | A6 | D6 | REG\_CT\_FOCUS\_AUTO | Focus, Auto. |
| 47 | 77 | A7 | D7 | REG\_CT\_IRIS\_ABSOLUTE | IRIS Absolute |
| 48 | 78 | A8 | D8 | REG\_CT\_IRIS\_RELATIVE | IRIS Relative. |
| 49 | 79 | A9 | D9 | REG\_CT\_ZOOM\_ABSOLUTE | Zoom Absolute |
| 4A | 7A | AA | DA | REG\_CT\_ZOOM\_RELATIVE | Zoom Relative |
| 4B | 7B | AB | DB | REG\_CT\_PANTILT\_ABSOLUTE | Pan-tilt Absolute |
| 4C | 7C | AC | DC | REG\_CT\_PANTILT\_RELATIVE | Pan-tilt Relative |
| 4D | 7D | AD | DD | REG\_CT\_ROLL\_ABSOLUTE | Roll Absolute |
| 4E | 7E | AE | DE | REG\_CT\_ROLL\_RELATIVE | Roll Relative |
| 4F | 7F | AF | DF | REG\_PU\_BACKLIGHT\_COMPENSATION | Backlight Compensation |
| 50 | 80 | B0 | E0 | REG\_PU\_BRIGHTNESS | Brightness |
| 51 | 81 | B1 | E1 | REG\_PU\_CONTRAST | Contrast |
| 52 | 82 | B2 | E2 | REG\_PU\_GAIN | Gain |
| 53 | 83 | B3 | E3 | REG\_PU\_POWER\_LINE\_FREQUENCY | Power line frequency |
| 54 | 84 | B4 | E4 | REG\_PU\_HUE | Hue |
| 55 | 85 | B5 | E5 | REG\_PU\_SATURATION | Saturation |
| 56 | 86 | B6 | E6 | REG\_PU\_SHARPNESS | Sharpness |
| 57 | 87 | B7 | E7 | REG\_PU\_GAMMA | Gamma |
| 58 | 88 | B8 | E8 | REG\_PU\_WHITE\_BALANCE\_TEMPERATURE | White Balance Temp. |
| 59 | 89 | B9 | E9 | REG\_PU\_WHITE\_BALANCE\_TEMPERATURE\_AUTO | White Balance Auto. |
| 5A | 8A | BA | EA | REG\_PU\_WHITE\_BALANCE\_COMPONENT | White Balance Component. |
| 5B | 8B | BB | EB | REG\_PU\_WHITE\_BALANCE\_COMPONENT\_AUTO | White Balance Component Auto. |
| 5C | 8C | BC | EC | REG\_PU\_DIGITAL\_MULTIPLIER | Digital Multiplier |
| 5D | 8D | BD | ED | REG\_PU\_DIGITAL\_MULTIPLIER\_LIMIT | Digital Multiplier Limit |
| 5E | 8E | BE | EE | REG\_PU\_HUE\_AUTO | Hue Auto. |
| 5F | 8F | BF | EF | REG\_PU\_ANALOG\_VIDEO\_STANDARD | Analog Video Standard. |

Table 2 - UVC Registers

|  |  |  |  |
| --- | --- | --- | --- |
| **Index** | **USB MODE** | **Resolution** | **Pixel Clock** |
| 1 | High Speed / Full Speed | QVGA | 27 MHz |
| 2 | Super Speed | VGA | 27 MHz |
| 3 | Super Speed | HD | 74.25 MHz |
| 4 | Super Speed | Full HD | 148.5 MHz |

Table 3 – Pixel Clock

# I2C Access

A user application can use the FTDI API FT\_I2CAccess to communicate with an I2C slave. The below code snippet shows a sample read operation.

i2c.addr = 0x0D; /\* I2C device address \*/

i2c.len = 2; /\* Length \*/

i2c.read\_access = TRUE; /\* Read \*/

i2c.reg = 0x13; /\* Offset to read \*/

i2c.reg\_is\_16\_bit = 0; /\* unused field…set to 0 \*/

FT\_I2CAccess(ftHandle, &i2c, (uint8\_t\*)&read\_value);

/\* read\_value returns the value read from the I2C Slave \*/

For more detailed information please refer to the sample code which can be found in the FT602 package.

## Interrupt notification.

A user application can also receive notifications based on certain events. I2C slave can utilize IRQ signal to notify the host. As seen in the figure 6, from the configuration programmer, after enabling the auxiliary interface, check the interrupt enable option.

A user application need to register a callback to receive interrupt notifications. The FTDI API FT\_SetNotificationCallback registers the callback for interrupt notification.

# Contact Information

|  |  |  |  |
| --- | --- | --- | --- |
| **Head Office – Glasgow, UK** | | **Branch Office – Tigard, Oregon, USA** | |
|  | |  | |
| Future Technology Devices International Limited  Unit 1, 2 Seaward Place, Centurion Business Park  Glasgow G41 1HH  United Kingdom  Tel: +44 (0) 141 429 2777  Fax: +44 (0) 141 429 2758 | | Future Technology Devices International Limited (USA)  7130 SW Fir Loop  Tigard, OR 97223-8160  USA  Tel: +1 (503) 547 0988  Fax: +1 (503) 547 0987 | |
|  | |  | |
| E-mail (Sales) | [sales1@ftdichip.com](mailto:sales1@ftdichip.com) | E-mail (Sales) | [us.sales@ftdichip.com](mailto:us.sales@ftdichip.com) |
| E-mail (Support) | [support1@ftdichip.com](mailto:support1@ftdichip.com) | E-mail (Support) | [us.support@ftdichip.com](mailto:us.support@ftdichip.com) |
| E-mail (General Enquiries) | [admin1@ftdichip.com](mailto:admin1@ftdichip.com) | E-mail (General Enquiries) | [us.admin@ftdichip.com](mailto:us.admin@ftdichip.com) |

|  |  |  |  |
| --- | --- | --- | --- |
| **Branch Office – Taipei, Taiwan** | | **Branch Office – Shanghai, China** | |
|  | |  | |
| Future Technology Devices International Limited (Taiwan)  2F, No. 516, Sec. 1, NeiHu Road  Taipei 114  Taiwan , R.O.C.  Tel: +886 (0) 2 8791 3570  Fax: +886 (0) 2 8791 3576 | | Future Technology Devices International Limited (China)  Room 1103, No. 666 West Huaihai Road,  Shanghai, 200052  China  Tel: +86 21 62351596  Fax: +86 21 62351595 | |
|  | |  | |
| E-mail (Sales) | [tw.sales1@ftdichip.com](mailto:tw.sales1@ftdichip.com) | E-mail (Sales) | [cn.sales@ftdichip.com](mailto:cn.sales@ftdichip.com) |
| E-mail (Support) | [tw.support1@ftdichip.com](mailto:tw.support1@ftdichip.com) | E-mail (Support) | [cn.support@ftdichip.com](mailto:cn.support@ftdichip.com) |
| E-mail (General Enquiries) | [tw.admin1@ftdichip.com](mailto:tw.admin1@ftdichip.com) | E-mail (General Enquiries) | [cn.admin@ftdichip.com](mailto:cn.admin@ftdichip.com) |

|  |  |
| --- | --- |
| **Web Site**  <http://ftdichip.com> |  |

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# Appendix A - References

## Document References

[FT602 IC Datasheet](http://www.ftdichip.com/Support/Documents/DataSheets/ICs/DS_FT600Q-FT601Q%20IC%20Datasheet.pdf)

[UMFT602x Datasheet](http://www.ftdichip.com/Support/Documents/DataSheets/Modules/DS_UMFT602x%20module%20datasheet.pdf)

[Altera Cyclone V](https://www.altera.com/products/fpga/cyclone-series/cyclone-v/overview.html)

## Acronyms and Abbreviations

|  |  |
| --- | --- |
| **Terms** | **Description** |
| FPGA | Field Programmable Gate Array |
| USB | Universal Serial Bus |
| UVC | USB Video Class |
| I2C | Inter-Integrated Circuit |
| API | Application Programming Interface |

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# Appendix C – Revision History

Document Title : AN\_434 FT602\_UVC\_Bus\_Master\_Sample

Document Reference No. : FT\_001392

Clearance No. :

Product Page : <http://www.ftdichip.com/FTProducts.htm>

Document Feedback : [Send Feedback](mailto:docufeedback@ftdichip.com?subject=Document%20Feedback:%20AN_434%20Version%201.1)

|  |  |  |
| --- | --- | --- |
| **Revision** | **Changes** | **Date** |
| Draft | Initial Release | 2017-11-24 |
|  |  |  |

**Revision History**

Revision history (internal use only, please clearly state all changes here before saving the file)

|  |  |  |  |
| --- | --- | --- | --- |
| **Revision** | **Date**  **YYYY-MM-DD** | **Changes** | **Editor** |

|  |  |  |  |
| --- | --- | --- | --- |
| Draft | 2017-11-24 | Initial Draft | Arun Pappan |