Future Technology Devices International Ltd.

Application Note

AN_146

USB Hardware Design Guidelines for FTDI ICs

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This document discusses several “best practices” to follow when designing with FTDI USB ICs.

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1 Introduction

While use of FTDI ICs makes USB easy to implement, care must be taken during the hardware design phase of a project to ensure certain practices are followed. This application note provides design guidelines for several common questions that have been asked of the FTDI Applications Engineering team. It is not a full and complete list of PCB design rules but only recommendations. It is expected that future releases of this application note will add further recommendations based on feedback from FTDI IC users.

1.1 Overview

USB was introduced in 1998 as a common means of attaching multiple types of peripherals to a personal computer. Since then, it has become the *de-facto* standard not only for personal computers but embedded systems as well. FTDI provides ICs for all of these USB applications. The topics throughout this application note endeavour to make the USB portion of a hardware design as easy as it is to use the functions of the FTDI ICs.

1.2 Scope

This application note covers USB hardware design as it relates to the FTDI USB ICs. It is not intended to be a comprehensive manual for USB in general. Where appropriate, references will be made to official USB Implementers Forum (USB-IF) documents. The USB-IF documentation should take precedence if there are any conflicts between official USB-IF documentation and this application note. A list of suggested devices is located in Appendix A – References.

Disclaimer – No warranty or guarantee is expressed or implied as to the suitability of the information contained within this application note. The product designer is responsible for any actions taken as a result of these comments.

2 USB Hardware Design Practices

2.1 Trace style (matched pair, controlled impedance, length)

USB requires two signals to make a single connection. For most data transfers, when one is high, the other is low. This is known as a differential pair. Other similar signalling styles are 10/100/1000BaseT Ethernet and RS485. All of these, including USB, require the use of twisted-pair cabling between devices. In particular, USB has specific shielding, signal and power conductor requirements. These requirements are identified in the USB 2.0 specification, Chapter 7.

At the PCB, the USB connector consists of 4 main signals: VBUS (+5V power), Ground and USB DP and DM. DP and DM are the differential pair. As with twisted pair cabling, these two signals must be closely matched with the following characteristics:

- *Equal length:* Both DP and DM signals must travel the same distance. If one trace ends up longer, then the timing of the signals can be adversely affected and cause data errors.
- *Controlled impedance:* The impedance of the twisted pair cabling must be matched on the PCB in order to minimize signal reflections. USB signals are 90Ω differential to each other / 45Ω each to Signal Ground. Most modern PCB layout software can be configured to route both of these signals together with these characteristics.
- *No stubs:* When adding components such as transient voltage protection or additional capacitance for edge rate control, the DP and DM signals should not have any "T"s in order to minimize signal reflections.
- *Ground planes:* With DP and DM being controlled impedance, they should consistently run over the USB Signal Ground plane. There should not be any splits in the plane directly under DP and DM.
- *Overall length:* The DP and DM signals should be made as short as possible. For very short runs, less than 1cm, it may not be possible to observe the controlled impedance specification. In practice, this is usually acceptable provided the other practices are followed.
- *General design practices:* Keep noisy sources away from the USB signals; avoid right angles; etc.

Figure 2.1 is taken from the "High Speed USB Platform Design Guide" by Intel and shows several common routing violations:

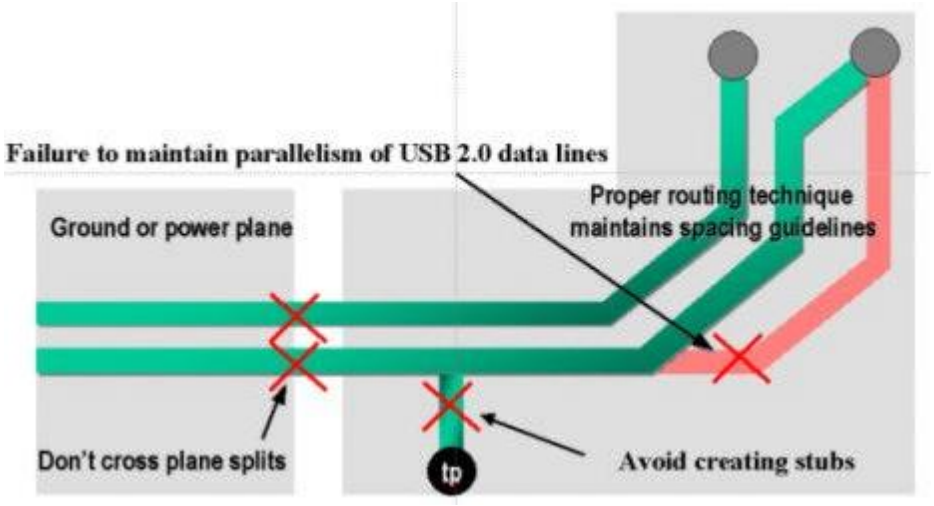

Figure 2.1 USB signal routing

2.2 Electrostatic protection, grounds, common mode chokes and isolation

2.2.1 Electrostatic Protection

FTDI ICs are tested for ESD protection between 2.5KV and 3KV. While this is sufficient for most embedded applications, it is often desirable to provide additional ESD protection on the USB DP, USB DM and VBUS signals, as shown in Figure 2.2.

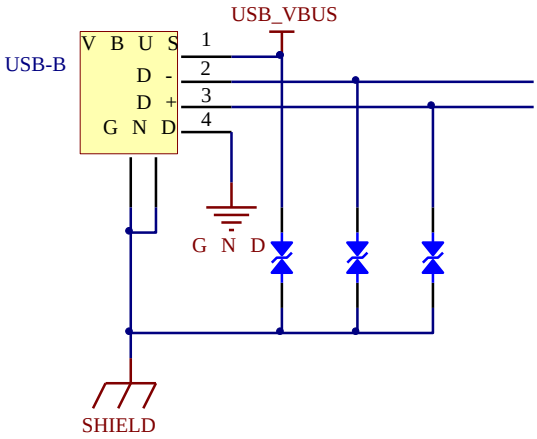

Figure 2.2 ESD protection on USB signals

It may also be desirable to add ESD protection for peripheral circuits that provide external connection points, such as a USB to RS232 adapter. Many line driver/level shifters have internal ESD protection to 15KV or more.

Transient suppressor devices should be placed as the first board-level device next to any external connection point (i.e. USB connector). This provides the shortest current path to ground, minimizing the possibility of damage elsewhere on the PCB.

2.2.2 Grounds

As noted above, USB consists of power, ground and two data signals. In addition, the USB connector provides connection to the shield on the USB cable. Over the years, FTDI have experienced that on designs where a standard USB A-B or A-miniB cable is in use, such as with the USB-COM232-Plus1, it is best to avoid directly connecting the USB shield and signal ground on the PCB. Provide pads for a zero-ohm resistor for a DC path or capacitor for a high-frequency path between shield and signal ground. This allows flexibility in the best component selection to minimize signal noise while providing EMC compatibility.

2.2.3 Common Mode Choke

Another means of controlling signal noise is though the use of a common mode choke. Care must be taken to select a component that is rated for USB2.0 operation. As with the matched and controlled impedance traces noted above, when using a common mode choke it is necessary that both USB signals are on a common core. The USB 2.0 specification notes that while acceptable, use of common mode chokes should be minimized.

2.2.4 Isolation

Finally, in applications where the peripheral is in an electrically noisy or potentially dangerous location, galvanic isolation may be provided. This can be done either at the USB interface, or on the peripheral side of the target circuit. Refer to FTDI Application Note AN_143 "Auto Sensing and Isolation Design for RS232/RS422/RS485 Interfaces" for examples of peripheral-side isolation. At the time of this writing,

FTDI are aware of only one manufacturer making an isolation device specifically designed for the USB bus.

2.3 Edge rate control

The timing of the rise/fall time of the USB signals is not only dependent on the USB signal drivers, it is also dependent system and is affected by factors such as PCB layout, external components and any transient protection present on the USB signals. For USB compliance these may require a slight adjustment. This timing can be modified through a programmable setting stored in the same external EEPROM that is used for the USB descriptors. Timing can also be changed by adding appropriate passive components to the USB signals:

- Capacitors may be placed on each of the USB DP and DM signals to ground. Note that the capacitance of any ESD suppressor must also be included in these values. Designers should take caution that adding too much capacitance may cause the USB transceiver to increase the drive strength, effectively defeating the intent of adding the capacitors.
    - 47pF / NPO/C0G dielectric for USB 2.0 Full-speed products (FT2xxB, FT2xxR, FT2xxX, FT2232D, VNC1L, VNC2)
    - 0 to 10pF / NPO/C0G dielectric for USB 2.0 Hi-speed products (FTx232H)
- Resistors may be placed in series with USB DP and DM.
    - 27Ω / 1% for FT2xxB, FT2xxX, FT2232D, FT12x, FT31xD and VNC2 *(series termination required for these families)*
    - 0Ω for FT2xxR and FT313H
    - 0Ω to 10Ω for FTx232H

Figure 2.3 shows typical placement of the termination and transient protection components.

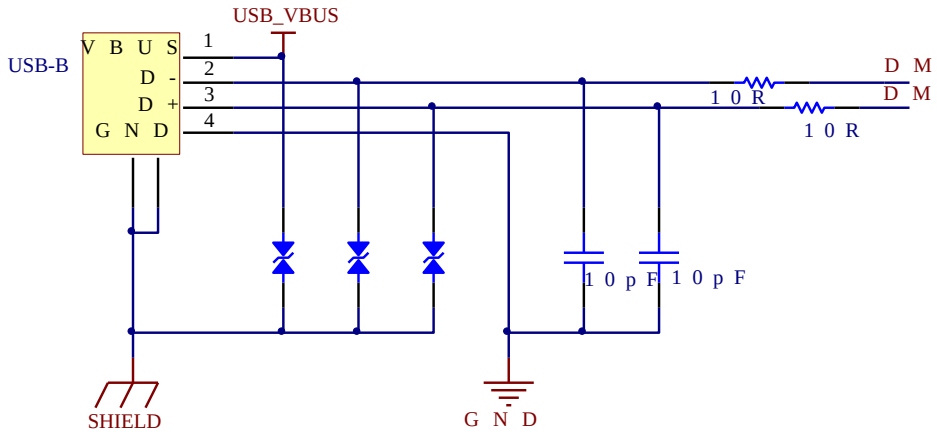

Figure 2.3 USB Termination

2.4 Power Requirements & Considerations

2.4.1 Power schemes – USB peripheral devices

USB peripheral devices can be configured in one of two settings:

- Bus-powered: The entire peripheral draws its power from the USB VBUS signal. The following restrictions apply:
    - Upon initial power-up prior to enumeration, a USB peripheral can draw no more than 100mA. If the peripheral draws no more than 100mA under all conditions, it is considered a low-power device.
    - After enumeration and power negotiation, a USB peripheral can draw no more than 500mA. A peripheral that draws between 100mA and 500mA is considered a high-power device.
    - When in USB suspend, a peripheral can draw up to 2.5mA if it is configured for remote wake capability. If the peripheral does not have remote wake capability, it can draw no more than 500µA in USB suspend. In order to pass USB-IF electrical certification, a peripheral configured for remote wake capability must provide a means of waking the system by an external event or signal.

- Self-powered:
  - Self-powered peripherals provide their own power supply. They do not draw any current from the USB bus.
  - Although a self-powered device does not require USB power while in suspend, it is still necessary to provide a means of waking the system if configured to do so.

Note that for all peripheral devices, no power may be back-fed into the USB VBUS signals under any circumstances

2.4.2 Bulk capacitance vs. inrush current – USB peripheral devices

For bus-powered peripherals, the USB 2.0 specification requires VBUS inrush current limiting equivalent to 10µF capacitance in parallel with a 44Ω load for the following conditions:

- Initial plug-in
- Upon enumeration and power negotiation of a high-power circuit
- Upon resuming from a sleep or suspend condition.

Larger bulk capacitance may be used, provided power is applied with a soft-start method so that the inrush specification is not exceeded. The FTDI FT-series ICs provide a Power Enable (PWREN#) signal to facilitate switching of a P-channel FET. An example soft-start RC circuit with PWREN# is shown in Figure 2.4.

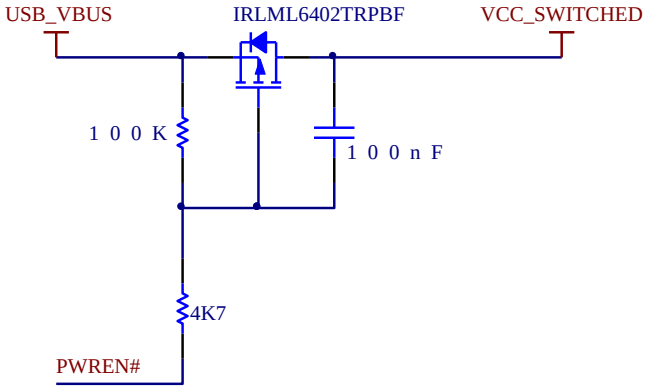

Figure 2.4 VBUS PWREN# Soft-Start

2.4.3 Over-current protection – USB peripheral devices

- Bus-powered: Although most upstream USB host and hub ports provide some form of over-current protection, it may be desirable to provide local protection as well.
- Self-powered: Circuit protection is recommended since the upstream USB port is not used for the power supply.
- Common methods are standard and resettable fuses. Inrush and normal operating current requirements will determine the fuse size.

2.4.4 Ferrite bead use and placement – USB peripheral devices

The USB specification prohibits the use of ferrite beads on the USB DP and DM data signals. It does, however, recommend them on the USB power signal (VBUS). It's common to add bulk and decoupling capacitors as shown in Figure 2.5:

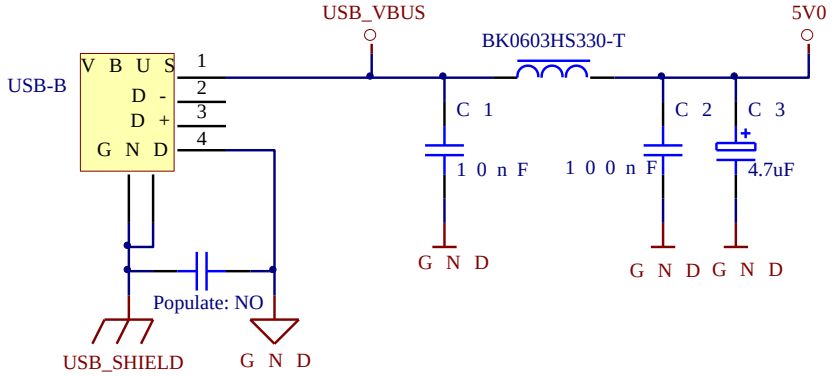

Figure 2.5 USB VBUS Filter

The 10nF capacitor and ferrite bead should be placed as close to the USB connector as possible.

Self powered peripherals typically do not require any filtering. Figure 2.6 shows the FTDI recommended method of holding the FT-series ICs in reset while a USB cable is not connected to the peripheral. If the IC is not held in reset, then the peripheral must provide a means of cycling RESET# when a cable is attached.

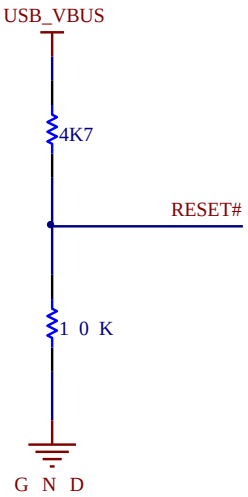

Figure 2.6 FT-Series Self-Powered Reset Circuit

2.4.5 USB Host Devices

FTDI manufacture a family of USB Host/Client devices called Vinculum. When used as a client device, all of the details listed above apply for a USB Full-speed peripheral device.

When used as a Host device, some additional details must be considered.

When designing an embedded USB host product, the design should take into account the power required by each bus-powered devices that may be attached. There are numerous USB power control products that can be controlled by GPIO signals and provide feedback whether a peripheral is attempting to consume excess current. At minimum, protection should be provided for at least 500mA of peripheral current.

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Distributor and Sales Representatives

Please visit the Sales Network page of the FTDI Website for the contact details of our distributor(s) and sales representative(s) in your country.

Appendix A – References

Document and Website References

Item	Description / Link
FTDI Documents	http://ftdichip.com/FTDocuments.htm Includes links to datasheets, application notes, solder profiles, PCB footprints, etc.
FTDI AN_143	Auto Sensing and Isolation Design for RS232/RS422/RS485 Interfaces
USB-COM232-Plus1 Datasheet	http://ftdichip.com/Documents/DataSheets/Modules/DS_USB-COM232-PLUS1.pdf
USB Implementers Forum	http://www.usb.org The primary source for all USB design information.
USB 2.0 Specification	http://www.usb.org/developers/docs/usb_20_052510.zip See Chapter 7 of the USB 2.0 specification for additional electrical details.
USB-IF Product List	http://www.usb.org/kcompliance/view A public list of products certified by the USB Implementers Forum.
"High Speed USB Platform Design Guidelines"	http://www.usb.org/developers/docs/hs_usb_pdg_r1_0.pdf This is a comprehensive discussion of USB PCB design guidelines and source for much of the discussion in this application note.

Acronyms and Abbreviations

Terms	Description
FET	Field Effect Transistor
PCB	Printed Circuit Board
PWB	Printed Wiring Board – same as PCB
TVS	Transient Voltage Suppressor
USB	Universal Serial Bus

Suggested Devices

Device	Description
TVS	Littelfuse PGB1010603 Semtech SRV05-4
Capacitors (small values)	Any brand NPO/C0G dielectric, 10% or better
Resistors	Any brand 1% or better
Ferrite Bead	Taiyo-Yuden BK0603HS330-T
FET	International Rectifier IRLML6402TRPBF
USB Full-Speed galvanic isolation	Analog Devices ADuM4160

Appendix B – List of Figures

Appendix C – Revision History

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Revision	Changes	Date
1.0	Initial Release	2010-06-04
1.1	Updated series termination information in Section 2.3 Updated US and CN Office addresses Updated formatting	2013-05-31
1.1	Version 1.1	2013-11-01

Revision Record Sheet

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Revision	Date	Details
1.0	2010-06-04	Initial Public Release
1.1	2013-05-31	Updated addresses, series termination info and formatting
1.1	2013-11-01	1.1 released

Sign Off

Signatory	Signature	Date
Managing Director		
Principal Hardware Engineer		
Principal Software Engineer		
Senior Marketing Manager		
Sales Manager		

Clearance Approval

- This Document is cleared for Future Technology Devices International use and unrestricted circulation.

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(Where applicable for external communications)

Revision History

Revision history (internal use only, please clearly state any changes here before saving the file)

Revision	Date YYYY-MM-DD	Changes	Editor
Draft	2010-05-26	Initial draft	Bob Recny
Draft	2010-05-27	Replaced ohm with Ω throughout Corrected suspend current to 500µA with no remote wake-up (p5)	Bob Recny
Draft	2010-05-28	Removed reference designators from all figures Added note on placement of TVSs (p4) Replaced edge rate description to match upcoming FTx232H datasheets (p4) Completed adding figures Completed Appendix A	Bob Recny
Draft	2010-05-31	Reviewed and comments added	Ian Dunn
Draft	2010-06-01	Updated sections 2.2.2, 2.2.4, 2.3 Rearranged section 2.4 subheadings and added one on fuses Changed section 2.5 to be a subheading of 2.4 Appendix A – added reference to AN_143, changed "recommended" to "suggested"	Bob Recny
1.0	2010-06-04	Final review and released to the web	Ian Dunn
1.1	2013-05-31	Updated series termination information in Section 2.3 Updated US and CN Office addresses Updated formatting	Bob Recny
1.1	2013-11-01	Approved LCE/DS	G Moore