Future Technology Devices International Ltd.

Application Note AN_139

Vinculum-II IO Mux Explained

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The purpose of this document is to describe the purpose and operation of the Vinculum-II (VNC2) IO Multiplexer (Mux) module.

TABLE OF CONTENTS

1 Introduction

The Vinculum VNC2 device is FTDI's 2nd generation USB host solution device and expands on the capabilities of the VNC1L. The device is supplied in 6 different packages. There are 32 pin QFN and LQFP packages, 48 pin QFN and LQFP packages and 64 pin QFN and LQFP packages.

The 32 pin packages have 12 IO pins, the 48 pin package has 28 IO pins and the 64 pin package has 44 IO pins.

Each of the IO pins interface to external logic and may be defined as an input or an output. All IO pins default to an input following a reset.

Following a reset, the IO MUX module within VNC2 can be configured to set the IO pin function and direction.

This application note describes what pin functions may be applied to the IO pins on each VNC2 package size. This will help when laying out an application PCB.

2 The IO Mux

The VNC2 IO Mux is based on 4 signal groupings – groups 1 to 3. The signals for each of the VNC2 interface modules ie UART, SPI slave, SPI master, FIFO, PWM or GPIO all belong to one of these 4 groups. Additionally each signal can only appear in one group and the groups are fixed.

2.1 Group 0 Signals and Available Pins

Available Input signals	Available output signals	64 Pin Package Available pins	48 Pin Package Available pins	32 Pin Package Available pins
debug_if fifo_data[0] fifo_data[4] fifo_oe# spi_s0_clk spi_s1_clk gpio[0] gpio[4] gpio[8] gpio[12] gpio[16] gpio[20] gpio[24] gpio[28] gpio[32] gpio[36]	debug_if uart_txd uart_dtr# uart_tx_active fifo_data[0] fifo_data[4] fifo_rxf# pwm[0] pwm[4] spi_m_clk spi_m_ss_1# gpio[0] gpio[4] gpio[8] gpio[12] gpio[16] gpio[20] gpio[24] gpio[28] gpio[32] gpio[36]	11, 15, 19, 24, 28, 39, 43, 47, 51, 57, 61	11, 15, 20, 31, 35, 41, 45	11, 23 29

Table 2.1: Group 0 Pins

This table shows that:

A design in a 32 pin package can select 3 signals from group 0
A design in a 48 pin package can select 7 signals from group 0
A design in a 64 pin package can select 11 signals from group 0

These signals can be a mixture of any of the available inputs or outputs shown in the table.

2.2 Group 1 Signals and Available Pins

Available Input signals	Available output signals	64 Pin Package Available pins	48 Pin Package Available pins	32 Pin Package Available pins
uart_rxd uart_dsr# fifo_data[1] fifo_data[5] spi_s0_mosi spi_s1_mosi gpio[1] gpio[5] gpio[9] gpio[13] gpio[17] gpio[21] gpio[25] gpio[29] gpio[33] gpio[37]	fifo_data[1] fifo_data[5] fifo_txe# pwm[1] pwm[5] spi_s0_mosi spi_s1_mosi spi_m_mosi fifo_clkout gpio[1] gpio[5] gpio[9] gpio[13] gpio[17] gpio[21] gpio[25] gpio[29] gpio[33] gpio[37]	12, 16, 20, 25, 29, 40, 44, 48, 52, 58, 62	12,16, 21, 32, 36, 42, 46	12, 24, 30

Table 2.2: Group 1 Pins

This table shows that:

A design in a 32 pin package can select 3 signals from group 1
A design in a 48 pin package can select 7 signals from group 1
A design in a 64 pin package can select 11 signals from group 1

These signals can be a mixture of any of the available inputs or outputs shown in the table.

2.3 Group 2 Signals and Available Pins

Available Input signals	Available output signals	64 Pin Package Available pins	48 Pin Package Available pins	32 Pin Package Available pins
uart_dcd# fifo_data[2] fifo_data[6] fifo_rd# spi_m_miso gpio[2] gpio[6] gpio[10] gpio[14] gpio[18] gpio[22] gpio[26] gpio[30] gpio[34] gpio[38]	uart_rts# fifo_data[2] fifo_data[6] pwm[2] pwm[6] spi_s0_miso spi_s1_miso gpio[2] gpio[6] gpio[10] gpio[14] gpio[18] gpio[22] gpio[26] gpio[30]	13, 17, 22, 26, 31, 41, 45, 49, 55, 59, 63	13, 18, 22, 33, 37, 43, 47	14, 25, 31

Table 2.3: Group 2 Pins

This table shows that:

A design in a 32 pin package can select 3 signals from group 2
A design in a 48 pin package can select 7 signals from group 2
A design in a 64 pin package can select 11 signals from group 2

These signals can be a mixture of any of the available inputs or outputs shown in the table.

2.4 Group 3 Signals and Available Pins

Available Input signals	Available output signals	64 Pin Package Available pins	48 Pin Package Available pins	32 Pin Package Available pins
uart_cts# uart_ri# fifo_data[3] fifo_data[7] fifo_wr# spi_s0_ss# spi_s1_ss# gpio[3] gpio[7] gpio[11] gpio[15] gpio[19] gpio[23] gpio[27] gpio[31] gpio[35] gpio[39]	fifo_data[3] fifo_data[7] pwm[3] pwm[7] spi_m_ss_0# gpio[3] gpio[7] gpio[11] gpio[15] gpio[19] gpio[23] gpio[27] gpio[31] gpio[35] gpio[39]	14, 18, 23, 27, 32, 42, 46, 50, 56, 60, 64	14, 19, 23, 34, 38, 44, 48	15, 26, 32

Table 2.4: Group 3 Pins

This table shows that:

A design in a 32 pin package can select 3 signals from group 3
A design in a 48 pin package can select 7 signals from group 3
A design in a 64 pin package can select 11 signals from group 3

These signals can be a mixture of any of the available inputs or outputs shown in the table.

3 Pin Selection

The first stage in selecting your pins is to identify the interfaces required for the application. Then determine the signals required for the interfaces and available pins.

UART	SPI_SLAVE0	SPI_SLAVE1	SPI_MASTER	FIFO	PWM	Debug
uart_txd	spi_s0_clk	spi_s1_clk	spi_m_clk	fifo_data[0]	pwm[0]	Debug_if
uart_rxd	spi_s0_ss#	spi_s1_ss#	spi_m_mosi	fifo_data[1]	pwm[1]	
uart_rts#	spi_s0_mosi	spi_s1_mosi	spi_m_miso	fifo_data[2]	pwm[2]	
uart_cts#	spi_s0_miso	spi_s1_miso	spi_m_ss0#	fifo_data[3]	pwm[3]	
uart_dtr#			spi_m_ss1#	fifo_data[4]	pwm[4]	
uart_dsr#				fifo_data[5]	pwm[5]	
uart_dcd#				fifo_data[6]	pwm[6]	
uart_ri#				fifo_data[7]	pwm[7]	
uart_tx_active				fifo_rxf#		
				fifo_txe#		
				fifo_rd#		
				fifo_wr		
				fifo_oe#[2]		
				Fifo_clkout[2]		

Table 3: Interface signals

1. Each pin can only be assigned one signal.
2. SYNC FIFO requires extra signals compared to ASYNC FIFO and is not available in 32 pin package – not enough pins.

After identifying the signals required, the user can refer to the tables in section 2 of this document to identify pins that the signal may be routed to.

For example, uart_txd is a member of Group 0 and is available on any of the group 0 pins not assigned to another signal.

3.1 IO Mux Defaults For Each Interface Module

The default pin assignment for each package when the IO Mux has been enabled, but no application has been configured is as follows:

Pin No. 64 Pin	Pin No. 48 Pin	Pin No. 32 Pin	Name	64 Pin Default	48 Pin Default	32 PIN Default	Type	Description
11	11	11	IOBUS0	debug_if	debug_if	debug_if	I/O	GPIO
12	12	12	IOBUS1	Input	pwm[1]	gpio[1]	I/O	GPIO
13	13	14	IOBUS2	Input	pwm[2]	gpio[2]	I/O	GPIO
14	14	15	IOBUS3	Input	pwm[3]	gpio[3]	I/O	GPIO
15	15	23	IOBUS4	fifo_data[0]	spi_s0_clk	uart_txd	I/O	GPIO
16	16	24	IOBUS5	fifo_data[1]	spi_s0_mosi	uart_rxd	I/O	GPIO
17	18	25	IOBUS6	fifo_data[2]	spi_s0_miso	uart_rts#	I/O	GPIO
18	19	26	IOBUS7	fifo_data[3]	spi_s0_ss#	uart_cts#	I/O	GPIO
19	20	29	IOBUS8	fifo_data[4]	spi_m_clk	spi_s0_clk	I/O	GPIO
20	21	30	IOBUS9	fifo_data[5]	spi_m_mosi	spi_s0_mosi	I/O	GPIO
22	22	31	IOBUS10	fifo_data[6]	spi_m_miso	spi_s0_miso	I/O	GPIO
23	23	32	IOBUS11	fifo_data[7]	spi_m_ss_0#	spi_s0_ss#	I/O	GPIO
24	31	-	IOBUS12	fifo_rxf#	uart_txd		I/O	GPIO
25	32	-	IOBUS13	fifo_txe#	uart_rxd		I/O	GPIO
26	33	-	IOBUS14	fifo_rd#	uart_rts#		I/O	GPIO
27	34	-	IOBUS15	fifo_wr#	uart_cts#		I/O	GPIO
28	35	-	IOBUS16	Input	uart_dtr#		I/O	GPIO
29	36	-	IOBUS17	Input	uart_dsr#		I/O	GPIO
31	37	-	IOBUS18	Input	uart_dcd#		I/O	GPIO
32	38	-	IOBUS19	Input	uart_ri#		I/O	GPIO
39	41	-	IOBUS20	uart_txd	uart_tx_active		I/O	GPIO
40	42	-	IOBUS21	uart_rxd	gpio[5]		I/O	GPIO
41	43	-	IOBUS22	uart_rts#	gpio[6]		I/O	GPIO
42	44	-	IOBUS23	uart_cts#	gpio[7]		I/O	GPIO
43	45	-	IOBUS24	uart_dtr#	gpio[0]		I/O	GPIO
44	46	-	IOBUS25	uart_dsr#	gpio[1]		I/O	GPIO
45	47	-	IOBUS26	uart_dcd#	gpio[2]		I/O	GPIO
46	48	-	IOBUS27	uart_ri#	gpio[3]		I/O	GPIO
47	-	-	IOBUS28	uart_tx_active			I/O	GPIO
48	-	-	IOBUS29	Input			I/O	GPIO
49	-	-	IOBUS30	Input			I/O	GPIO
50	-	-	IOBUS31	Input			I/O	GPIO
51	-	-	IOBUS32	spi_s0_clk			I/O	GPIO
52	-	-	IOBUS33	spi_s0_mosi			I/O	GPIO
55	-	-	IOBUS34	spi_s0_miso			I/O	GPIO
56	-	-	IOBUS35	spi_s0_ss#			I/O	GPIO
57	-	-	IOBUS36	spi_s1_clk			I/O	GPIO
58	-	-	IOBUS37	spi_s1_mosi			I/O	GPIO
59	-	-	IOBUS38	spi_s1_miso			I/O	GPIO
60	-	-	IOBUS39	spi_s1_ss#			I/O	GPIO
61	-	-	IOBUS40	spi_m_clk			I/O	GPIO
62	-	-	IOBUS41	spi_m_mosi			I/O	GPIO
63	-	-	IOBUS42	spi_m_miso			I/O	GPIO
64	-	-	IOBUS43	spi_m_ss_0#			I/O	GPIO

Table 3.1: IO Mux Defaults for each interface module

3.2 Additional Pin Information

- Each signal can be routed to more than one pin. This may be useful for sniffing output data for debug e.g. UART _TXD.
- Unused interface modules do not need to reserve pins. For example, if the UART interface is not enabled then it is not necessary to reserve pins for the UART function. The pins that are reserved for UART by default would default to GPIO inputs.
- It is not essential to reserve a pin for the debug interface but may be advisable for debug and chip programming purposes.

4 Summary

Although the VNC2 IO Mux seems complex, it provides maximum flexibility in selection of interface types. This document attempts to explain how to use this function.

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Appendix A– Revision History

Version Draft	First Draft	10/02/2010
Version 1.0	First Release	19/02/2010