Technical Note

TN_158

What is the Camera Parallel Interface?

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This technical note explains the basics of the Camera Parallel Interface, a feature of FTDI MCUs.

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1 Introduction

Many embedded systems benefit from the use of a camera. An embedded camera is typically comprised of three parts: lens assembly, image sensor(s) and the digital interface.

Over the years, the MIPI Alliance have specified successive camera digital interfaces: Camera Parallel Interface (CPI), Camera Serial Interface 1 (CSI-1), Camera Serial Interface 2 (CSI-2), and Camera Serial Interface 3 (CSI-3). This technical note focuses on the CPI.

Although the MIPI Alliance (www.mipi.org) claims there is no acronym associated with "MIPI", it is often referred to as the "Mobile Industry Processor Interface".

The MIPI Specification is a set of standards adopted by the MIPI Alliance for various mobile product functions.

2 Camera Parallel Interface

An image sensor captures images at a particular rate and makes the corresponding data available through one of several digital interfaces. Shown here is the OmniVision OV7675 VGA sensor:

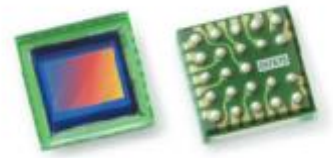

Figure 2.1 - Typical Image Sensor

Image sensors are coupled with a lens to become a camera module. The camera modules can then be mounted in an assembly.

Shown here is the OmniVision OVM7692 CameraCubeChip™ – a complete camera module with the Camera Parallel Interface:

Figure 2.2 - Typical Camera Module

The CPI is one of the original image sensor interfaces specified by the MIPI Alliance. It consists of two portions: an I^2C bus to control the interface and a parallel bus for the image data itself.

2.1 Signals

2.1.1 I^2C Control Signals

The I^2C bus is used in many applications, such as a personal computer System Management Bus to identify and control various features of the system. It is also used for monitoring and control of different devices. In this case, the I^2C bus is used to control the various registers of the camera module.

The I^2C bus consists of two signals: SDA (data) and SCK (clock). The I^2C signals are connected in a daisy-chain multi-drop configuration. An MCU provides the I^2C master used to communicate with the camera configuration interface. The typical interface voltage of a camera module is 1.5V to 2.8V. Each signal is driven in an open-drain configuration where only logic zeroes are transmitted. A logic 1 relies on the pull-up resistor on the bus. Multiple devices can be connected to a single bus in a daisy-chain, multi-drop configuration.

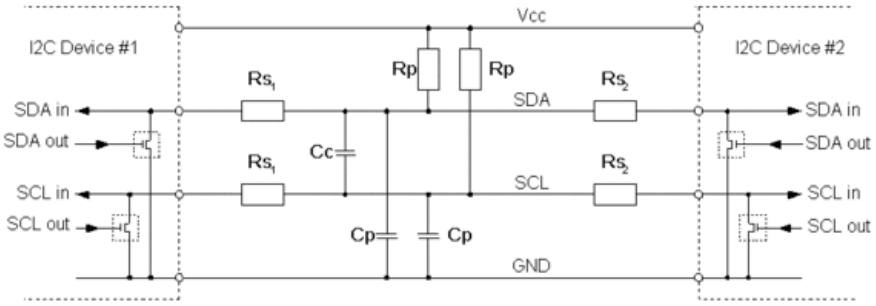

Image from www.i2c-bus.org

Figure 2.3 - Typical I²C connection

A common 7-bit or 10-bit addressing scheme is used by the I²C master to identify and select a particular I²C slave for communication.

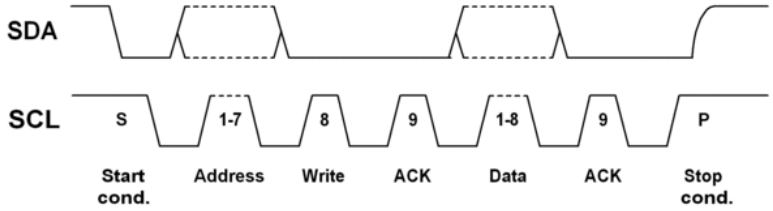

Image from www.i2c-bus.org

Figure 2.4 - I²C signaling

2.1.2 Parallel Data Signals

An 8-bit parallel link connects to the video data bus from an image sensor. The sensor also provides Vertical SYNC (VSYNC), Horizontal Reference (HREF) and Pixel clock (PCLK) timing signals. The parallel interface is unidirectional. All parallel signals are transmitted by the camera module and received by the controlling MCU.

Image data is output for each rising edge of PCLK. HREF is high while clocking out active image data for each scan line. VSYNC is pulsed high at the start of each frame. Refer to the camera module datasheet for timing specifications for these signals.

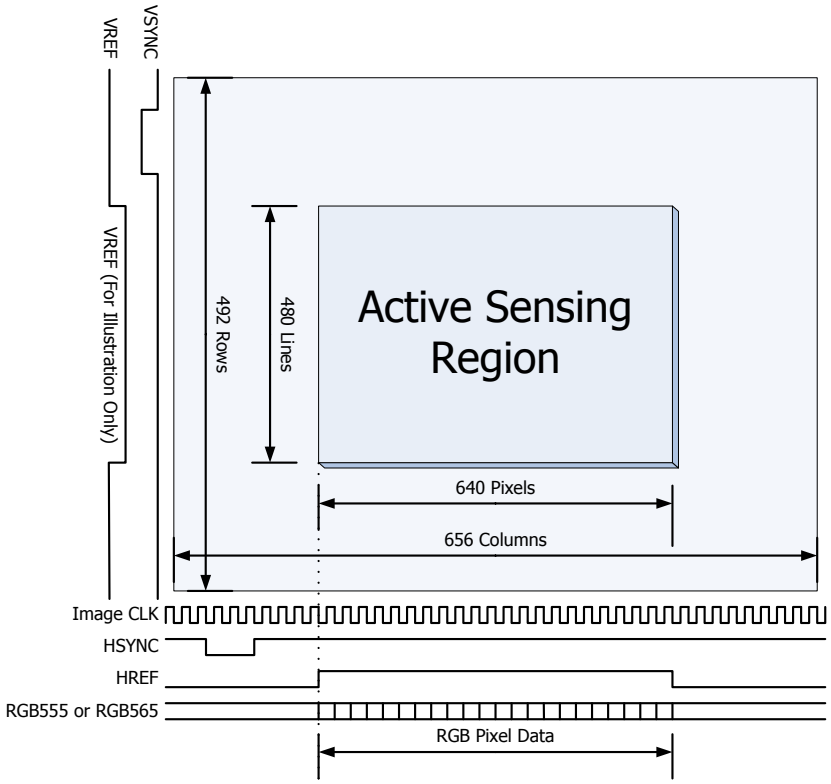

Figure 2.5 - Typical Parallel Interface Timing

The figure above shows how the signals are related. A "VREF" signal is shown for illustration, though it is not an actual signal output from the sensor. The image clock is one clock per pixel. The actual PCLK is 2x the frequency since the data for each pixel consists of 16-bits being clocked on an 8-bit interface. The actual number of columns and rows will vary with each different sensor or camera module. Refer to the device's datasheet for the actual values.

2.2 Typical Interconnect

Both I^2C and parallel portions of the CPI will connect to a MCU that supports the interface (SDA, SCL, D7:0, PCLK, VSYNC, and HREF). The voltage levels required at each end of the interface may indicate the need for level shifters. The image below shows the connections.

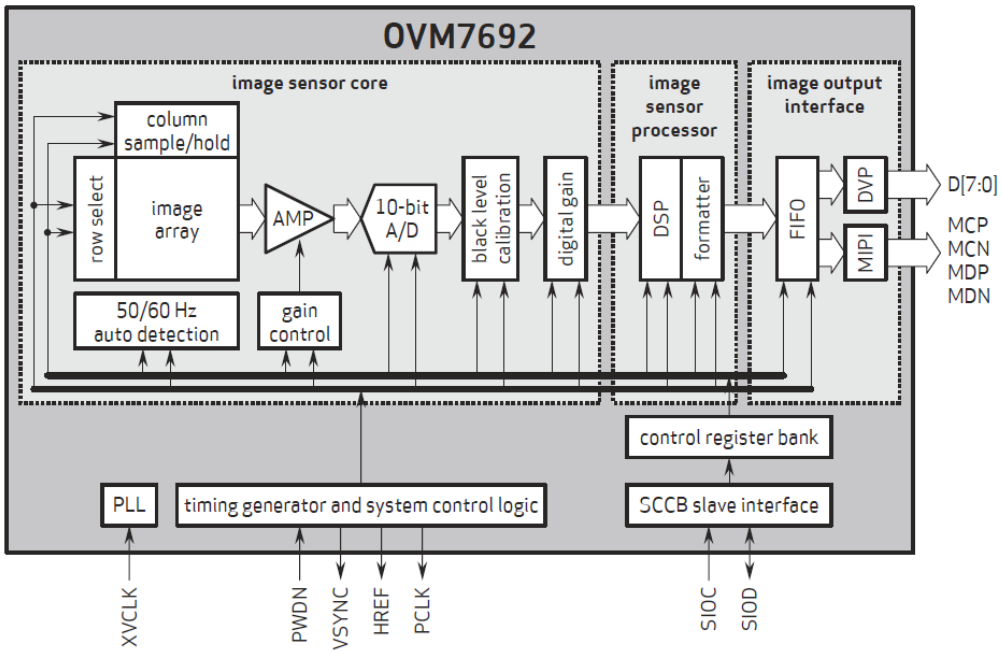

Image from OmniVision OVM7692 Product Brief

Figure 2.6 - Typical Image Sensor Block Diagram

The MCP, MCN, MDP and MDN signals are not used in the case of the CPI. SIOC and SIOD are the I^2C SCL and SDA, respectively.

2.3 Data Format

There are several ways that camera modules format the data. One common method is to output the data in a packed pixel 2-byte format. RGB565 (16-bit) and RGB555 (15-bit) modes are shown here:

Mode	Byte	D7	D6	D5	D4	D3	D2	D1	D0
RGB565	First	R4	R3	R2	R1	R0	G5	G4	G3
	Second	G2	G1	G0	B4	B2	B2	B1	B0
RGB555	First	X	R4	R3	R2	R1	R0	G4	G3
	Second	G2	G1	G0	B4	B2	B2	B1	B0

Table 2.1 - Color Encoding on Pixel Data

Each image point takes two clocks to send the full pixel data to the MCU. For 16-bit encoding, 65,536 colors can be represented. For 15-bit encoding, 32,768 colors can be represented.

Other formats may be available as well. Some only require one byte per pixel; however, the color depth will be limited. YUV422 is one of these formats. Data information is conveyed in luminance and chrominance rather than direct red, green and blue.

2.4 Frame rates

A single scan of a frame can take a snapshot or still image. When looking at streaming video, the frame rate becomes important. A full frame consists of the entire image including the leading and

trailing sections beyond the active image area – the "front porch" and "back porch" in analog video terminology. Referring to Figure 2.5, the overall frame is 656x492 for the 640x480 image. Each pixel takes two PCLK cycles – one for each byte – so the number of pixel clocks to capture a full frame is:

$$656\ (horizontal) * 492\ (vertical) * \frac{2\ bytes}{pixel} = 645504\ PCLK\ cycles\ per\ frame$$

For a theoretical maximum PCLK rate of 25MHz, the maximum number of frames per second is:

$$\frac{25MHz}{645504\ PCLK\ per\ frame} = 38.7\ frames\ per\ second\ (fps)$$

In generic terms:

$$Theoretical\ Frame\ Rate = \frac{Maximum\ supported\ PCLK}{Horizontal\ size * Vertical\ size * \frac{Bytes}{pixel}}$$

In practice, the actual frame rate is usually slower due to the MCU processing of the incoming data.

2.5 Other Image Sensor and Camera Interfaces

The CPI is not unlike a parallel LCD interface. Both have a pixel clock, pixel data, and horizontal and vertical reference signals. Data direction is the primary difference. The image sensor/camera module sends data to the MCU while the LCD displays data from the MCU (or video controller).

The MIPI Alliance also have defined Camera Serial Interfaces, denoted CSI-1, CSI-2, or CSI-3. The I^2C portion remains. The parallel portion is replaced differential clock and data signals. CSI-1 has a single data pair and a single clock pair. CSI-2 can provide multiple data pairs. CSI-3 is an extension of CSI-2 and accounts for additional protocol specifications and EMI concerns.

3 Typical Applications

There are many applications for embedded cameras and image sensors. The CPI and CSI interfaces provide a well-defined interface for connection of these image devices to a MCU. Some examples of where camera data is useful include:

- Security systems and surveillance
- Child monitors
- Production inspection systems
- Image recognition
- Mobile phones
- Internet connected camera
- Manned or unmanned aircraft
- Police & fire (vehicle dash-cam or on-person video recording)

4 What FTDI Offer

FTDI now offers the FT900 series microcontrollers that provide a connection for image sensors over the industry standard MIPI Camera Parallel Interface (CPI). Full VGA (640x480) at up to 15fps can be achieved with the FT900 series camera interface. Higher rates are possible with smaller images.

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Appendix A – References

Document References

FT900 Datasheet

I²C bus

MIPI Alliance

MIPI Camera Interfaces

OmniVision sensor with parallel interface (OV7675)

OmniVision CameraCubeChip camera module with parallel interface (OVM7962)

Acronyms and Abbreviations

Terms	Description
CPI	Camera Parallel Interface
CSI	Camera Serial Interface
HREF	Horizontal Reference
MIPI	MIPI Alliance (MIPI itself is not an acronym)
PCLK	Pixel Clock
VSYNC	Vertical Sync

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