Future Technology Devices International Ltd

FT4233H

(High Speed USB Bridge with Type-C/PD Controller)

The FT4233H is a Hi-Speed USB device with a Type-C/PD controller that fully supports the latest USB Type-C and Power Delivery (PD) standards enabling support for power negotiation with the ability to sink or source current to a USB host device. The USB bridge function delivers 4 independent channels compatible with the FT4232H – Quad Hi-speed USB to multipurpose UART/MPSSE solution.

The FT4233H has the following advanced features:

- Support PD specification Rev 3.0.
- Port1 mode configuration for Sink or Dual-role, supporting Fast Role Swap
- Port2 works as Sink, supporting charge through to port1
- Support 5V, 9V, 15V and 20V PDOs as sink or source
- Type-C/PD Physical Layer Protocol
- PD policy engine using 32-bit RISC controller with 8kB data RAM and 48kB code ROM
- Support PD capability descriptors and requests
- Options to use external MCU controlling PD policy through I2C interface
- USB to quad serial ports with a variety of configurations.
- Entire USB protocol handled on the chip. No USB specific firmware programming required.
- USB 2.0 High Speed (480Mbits/Second) and Full Speed (12Mbits/Second) compatible.
- Two Multi-Protocol Synchronous Serial Engine (MPSSE) on channel A and channel B, to simplify synchronous serial protocol (USB to JTAG, I^2C, SPI or bit-bang) design.
- Independent Baud rate generators.
- RS232/RS422/RS485 UART Transfer Data Rate up to 12Mbaud. (RS232 Data Rate limited by external level shifter).
- FTDI's royalty-free Virtual Com Port (VCP) and Direct (D2XX) drivers eliminate the requirement for USB driver development in most cases.
- Optional traffic TX/RX indicators can be added with LEDs and an external 74HC595 shift register.
- Adjustable receive buffer timeout.
- Support for USB suspend and resume conditions via PWREN#, SUSPEND# and RI# pins.
- FTDI FT232B style, asynchronous serial UART interface option with full hardware handshaking and modem interface signals.
- Fully assisted hardware or X-On / X-Off software handshaking.
- UART Interface supports 7/8 bit data, 1/2 stop bits, and Odd/Even/Mark/Space/No Parity.
- Auto-transmit enable control for RS485 serial applications using TXDEN pin.
- Operational configuration mode and USB Description strings configurable in external EEPROM over the USB interface.
- Low operating and USB suspend current.
- Configurable I/O drive strength (4, 8, 12 or 16mA) and slew rate.
- Supports bus powered, self-powered and high-power bus powered USB configurations.
- USB Bulk data transfer mode (512 byte packets in High Speed mode).
- Dedicated Windows DLLs available for USB to JTAG, USB to SPI, and USB to I^2C applications.
- +3.3V single supply operating voltage range.
- +3.3V I/O interfacing.
- Highly integrated design includes +1.2V LDO regulator for VCORE, integrated POR function and on chip clock multiplier PLL (12MHz – 480MHz).
- Extended -40°C to 85°C industrial operating temperature range.
- Available in Pb-free QFN-76 package (RoHS compliant)

1 Typical Applications

- USB bridge with Type-C/PD charge through
- High-power application from USB Type-C port (up to 100W)
- Single chip USB to four channels UART (RS232, RS422 or RS485) or Bit-Bang interfaces.
- Single chip USB to 2 JTAG channels plus 2 UARTS.
- Single chip USB to 1 JTAG channel plus 3 UARTS.
- Single chip USB to 1 SPI channel plus 3 UARTS.
- Single chip USB to 2 SPI channels plus 2 UARTS.
- Single chip USB to 2 Bit-Bang channels plus 2 UARTS.
- Single chip USB to 1 SPI channel, plus 1 JTAG channel plus 2 UARTS.
- Single chip USB to 2 I^2C channels plus 2 UARTS.
- Numerous combinations of 4 channels.
- Upgrading Legacy Peripheral Designs to USB
- Field Upgradable USB Products
- Cellular and cordless phone USB data transfer cables and interfaces.
- Interfacing MCU / PLD / FPGA based designs to USB
- PDA to USB data transfer
- USB Smart Card Readers
- USB Instrumentation
- USB Industrial Control
- USB MP3 Player Interface
- USB FLASH Card Reader / Writers
- Set Top Box PC - USB interface
- USB Digital Camera Interface
- USB Bar Code Readers

1.1 Driver Support

The FT4233H requires USB drivers (listed below), available free from http://www.ftdichip.com, which are used to make the FT4233H appear as a virtual COM port (VCP). This allows the user to communicate with the USB interface via a standard PC serial emulation port (for example TTY). Another FTDI USB driver, the D2XX driver, can also be used with application software to directly access the FT4233H through a DLL.

Royalty free VIRTUAL COM PORT (VCP) DRIVERS for...

- Windows 10 32,64-bit
- Windows 8/8.1 32,64-bit
- Windows 7 32,64-bit
- Windows Server 2008 and server 2012 R2
- Mac OS-X
- Linux 2.4 and greater

Royalty free D2XX *Direct* Drivers (USB Drivers + DLL S/W Interface)

- Windows 10 32,64-bit
- Windows 8/8.1 32,64-bit
- Windows 7 32,64-bit
- Windows Server 2008 and server 2012 R2
- Linux 2.4 and greater
- Android(J2xx)

For driver installation, please refer to the installation guides on our website:
http://www.ftdichip.com/Support/Documents/InstallGuides.htm

The following additional installation guides application notes and technical notes are also available:

- AN_113, "Interfacing FT2232H Hi-Speed Devices To I2C Bus".
- AN_109 – "Programming Guide for High Speed FTCI2C DLL"
- AN_110 – "Programming Guide for High Speed FTCJTAG DLL"
- AN_111 – "Programming Guide for High Speed FTCSPI DLL"
- AN 113 – "Interfacing FT2232H Hi-Speed Devices To I2C Bus"
- AN114 – "Interfacing FT2232H Hi-Speed Devices To SPI Bus"
- AN135 – MPSSE Basics
- AN108 - Command Processor For MPSSE and MCU Host Bus Emulation Modes
- TN_104, "Guide to Debugging Customers Failed Driver Installation"

1.2 Part Numbers

Part Number	Package
FT4233HQ-xxxx	76 Pin QFN

2 FT4233H Block Diagram

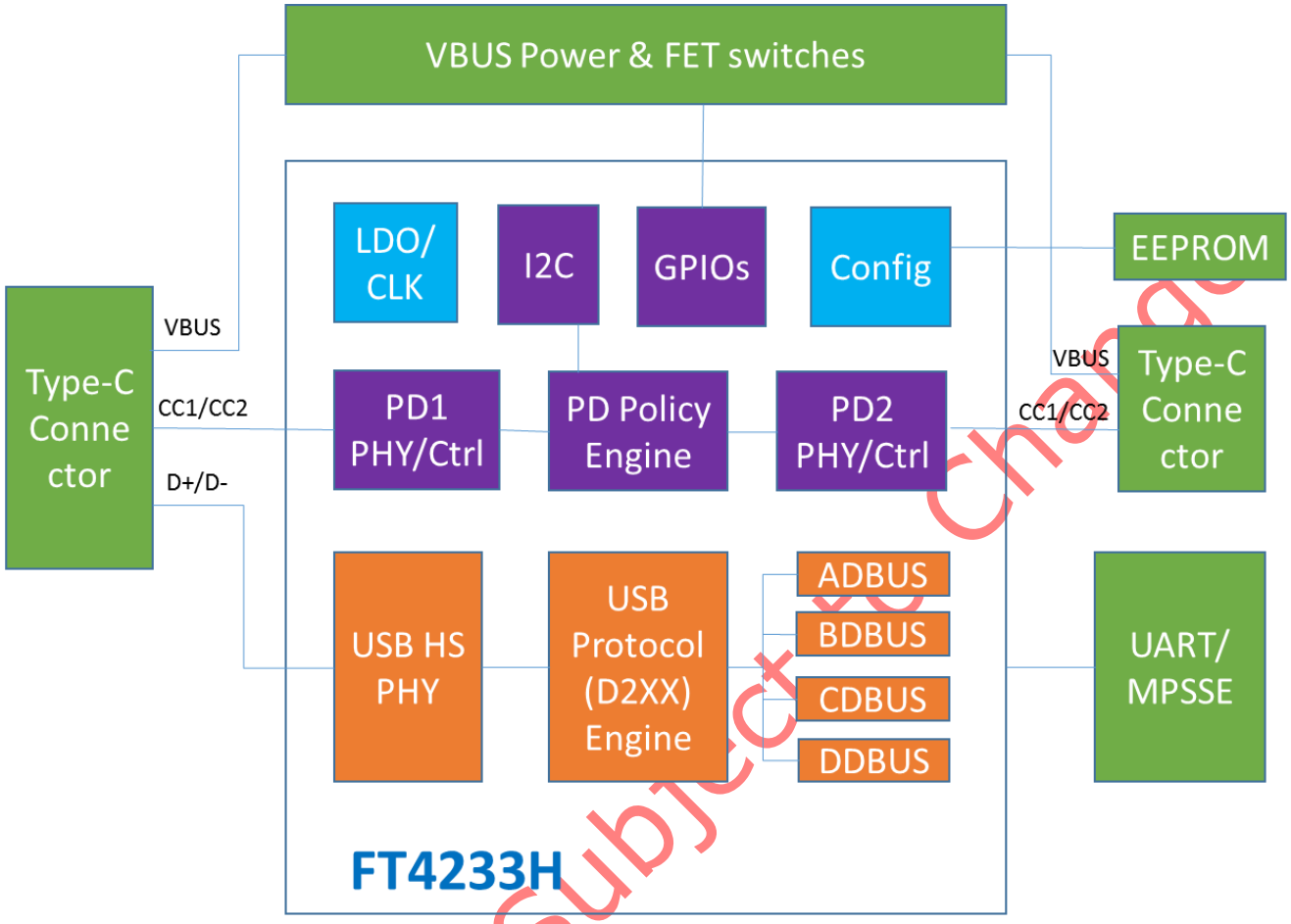

Figure 2.1 FT4233H Block Diagram

For a description of each function please refer to Section 4.

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3 Device Pin Out and Signal Description

3.1 Pin Configurations

This section describes the operation of the FT4233H pins. The function of many pins is determined by the configuration of the FT4233H. The following table details the function of each pin dependent on the configuration of the interface. Each of the functions is described in

Table 3.1.

Note: The convention used throughout this document for active low signals is the signal name followed by #

FT4233HQ (76-pin)					
Pins		**Pin functions (depend on configuration)**			
Pin #	Pin Name	ASYNC Serial (RS232)	ASYNC Bit-bang	SYNC Bit-bang	MPSSE
Channel A					
9	ADBUS0	TXD	D0	D0	TCK/SK
10	ADBUS1	RXD	D1	D1	TDI/DO
11	ADBUS2	RTS#	D2	D2	TDO/DI
12	ADBUS3	CTS#	D3	D3	TMS/CS
15	ADBUS4	DTR#	D4	D4	GPIOL0
16	ADBUS5	DSR#	D5	D5	GPIOL1
17	ADBUS6	DCD#	D6	D6	GPIOL2
18	ADBUS7	RI#/ TXDEN*	D7	D7	GPIOL3
Channel B					
19	BDBUS0	TXD	D0	D0	TCK/SK
20	BDBUS1	RXD	D1	D1	TDI/DO
22	BDBUS2	RTS#	D2	D2	TDO/DI
23	BDBUS3	CTS#	D3	D3	TMS/CS
24	BDBUS4	DTR#	D4	D4	GPIOL0
25	BDBUS5	DSR#	D5	D5	GPIOL1
26	BDBUS6	DCD#	D6	D6	GPIOL2
27	BDBUS7	RI#/ TXDEN*	D7	D7	GPIOL3
Channel C					
36	CDBUS0	TXD	D0	D0	RS232 or Bit-Bang interface
37	CDBUS1	RXD	D1	D1	RS232 or Bit-Bang interface
38	CDBUS2	RTS#	D2	D2	RS232 or Bit-Bang interface
39	CDBUS3	CTS#	D3	D3	RS232 or Bit-Bang interface
40	CDBUS4	DTR#	D4	D4	RS232 or Bit-Bang interface
42	CDBUS5	DSR#	D5	D5	RS232 or Bit-Bang interface
43	CDBUS6	DCD#	D6	D6	RS232 or Bit-Bang interface
44	CDBUS7	RI#/ TXDEN*	D7	D7	RS232 or Bit-Bang interface
Channel D					
48	DDBUS0	TXD	D0	D0	RS232 or Bit-Bang interface
49	DDBUS1	RXD	D1	D1	RS232 or Bit-Bang interface
50	DDBUS2	RTS#	D2	D2	RS232 or Bit-Bang interface
51	DDBUS3	CTS#	D3	D3	RS232 or Bit-Bang interface
52	DDBUS4	DTR#	D4	D4	RS232 or Bit-Bang interface
53	DDBUS5	DSR#	D5	D5	RS232 or Bit-Bang interface
55	DDBUS6	DCD#	D6	D6	RS232 or Bit-Bang interface
57	DDBUS7	RI#/ TXDEN*	D7	D7	RS232 or Bit-Bang interface

Table 3.1 FT4233H Pin Configurations

***** RI#/ or TXDEN is selectable in the EEPROM. Default is RI#.

3.2 Common Pins

The operation of the following FT4233H pins are the same regardless of the configured mode:-

Pin No.	Name	Type	Description
13,29,47,74	VCORE	POWER Input	+1.2V input. Core supply voltage input. Connect to pin 33 when using internal regulator.
7,21,41,54	VCCIO	POWER Input	+3.3V input. I/O interface power supply input. Failure to connect all VCCIO pins will result in failure of the device.
62	VCC_USB	POWER Input	+3.3V Input. Internal USB PHY power supply input. Note that this cannot be connected directly to the USB supply. A +3.3V regulator must be used. It is recommended that this supply is filtered using an LC filter.
66	VCC_PD	POWER Input	+3.3V Input. Internal PD PHY power supply input.
32	VREGIN	POWER Input	+3.3V Input. Integrated 1.2V voltage regulator input.
33	VREGOUT	POWER Output	+1.2V Output. Integrated voltage regulator output. Connect to VCORE with 3.3uF filter capacitor.
34	FSOURCE	POWER Input	FSOURCE input pin for EFUSE. Leave float for normal operation
35	VPP	POWER Input	VPP input pin for EFUSE. Leave float for normal operation
14,28,56, centre die pad	GND	POWER Input	Ground.

Table 3.2 FT4233H Power and Ground Pins

Pin No.	Name	Type	Description
31	OSCI	INPUT	Oscillator input.
30	OSCO	OUTPUT	Oscillator output.
65	REF	INPUT	Current reference – connect via a 12K Ohm resistor @ 1% to GND.
63	DM	I/O	USB Data Signal Minus.
64	DP	I/O	USB Data Signal Plus.
3	TEST	INPUT	IC test pin – for normal operation should be connected to GND.
4	RESET#	INPUT	Reset input (active low).
75	PWREN#	OUTPUT	Active low power-enable output. PWREN# = 0: Normal operation.

			PWREN# =1: USB SUSPEND mode or device has not been configured. This can be used by external circuitry to power down logic when device is in USB suspend or has not been configured.
45	SUSPEND#	OUTPUT	Active low when USB is in suspend mode.

Table 3.3 Common Function pins

Pin No.	Name	Type	Description
76	EECS	I/O	EEPROM – Chip Select. Tri-State during device reset.
1	EECLK	OUTPUT	Clock signal to EEPROM. Tri-State during device reset. When not in reset, this outputs the EEPROM clock.
2	EEDATA	I/O	EEPROM – Data I/O Connect directly to Data-In of the EEPROM and to Data-Out of the EEPROM via a 2.2K resistor. Also, pull Data-Out of the EEPROM to VCC via a 10K resistor for correct operation. Tri-State during device reset.

Table 3.4 EEPROM Interface pins

Pin No.	Name	Type	Description
68	PD1_SVBUS	AI	Analog input. Scaled down VBUS sensing input for PD1. VBUS is required to be divided by 10 before input to this pin.
69	PD1_VCONN	Power Input	Power input for PD1 VCONN power source. Connect to 3.3V.
70	PD1_CC1	AI/O	Analog IO pin. PD1 CC1 pin
67	PD1_CC2	AI/O	Analog IO pin. PD1 CC1 pin
72	PD2_SVBUS	AI	Analog input. Scaled down VBUS sensing input for PD2. VBUS is required to be divided by 10 before input to this pin.
71	PD2_CC1	AI/O	Analog IO pin. PD2 CC1 pin
73	PD2_CC2	AI/O	Analog IO pin. PD2 CC1 pin

Table 3.5 Type-C/PD port pins

Pin No.	Name	Type	Description
68	GPIO0	I/O	GPIO0 or I2C_SDA pin. Default function is GPIO0 input with weak pull-down.
69	GPIO1	I/O	GPIO1 or I2C_SCL pin. Default function is GPIO1 input with weak pull-down.
70	GPIO2	I/O	GPIO2 or I2C_INT# pin. Default function is GPIO2 input with weak pull-down.
67	GPIO3	I/O	GPIO3 pin. Default function is GPIO3 input with weak pull-down.
72	GPIO4	I/O	GPIO4 pin. Default function is GPIO4 input with weak pull-down.
71	GPIO5	I/O	GPIO5 pin. Default function is GPIO5 input with weak pull-down.
73	GPIO6	I/O	GPIO6 pin. Default function is GPIO6 input with weak pull-down.
73	GPIO7	I/O	GPIO7 pin. Default function is GPIO7 input with weak pull-down.

Table 3.6 GPIO pins

3.3 Configured Pins

The following sections describe the function of the configurable pins referred to in

Table 3.1 which is determined by how the FT4233H is configured.

3.3.1 FT4233H Pins used as an Asynchronous Serial Interface

Any of the 4 channels of the FT4233H can be configured as an asynchronous serial UART interface (RS232/422/485). When configured in this mode, the pins used and the descriptions of the signals are shown in **Table 3.7**.

Name	Type	RS232 Configuration Description
TXD	OUTPUT	TXD = transmitter output
RXD	INPUT	RXD = receiver input
RTS#	OUTPUT	RTS# = Ready To send handshake output
CTS#	INPUT	CTS# = Clear To Send handshake input
DTR#	OUTPUT	DTR# = Data Transmit Ready modem signaling line
DSR#	INPUT	DSR# = Data Set Ready modem signaling line
DCD#	INPUT	DCD# = Data Carrier Detect modem signaling line
RI#/ TXDEN	INPUT/OUTPUT	RI# = Ring Indicator Control Input. When the Remote Wake-Up option is enabled in the EEPROM, taking RI# low can be used to resume the PC USB Host controller from suspend. (see note 1, 2 and 3) TXDEN = (TTL level). For use with RS485 level converters.

Table 3.7 Channel A, B, C and D Asynchronous Serial Interface Configured Pin Descriptions

Notes

1. When using remote wake-up, ensure the resistors are pulled-up in suspend. Also ensure peripheral designs do not allow any current sink paths that may partially power the peripheral.
2. If remote wake-up is enabled, a peripheral is allowed to draw up to 2.5mA in suspend. If remote wake-up is disabled, the peripheral must draw no more than 500uA in suspend.
3. If a Pull-down is enabled, the FT4233H will not wake up from suspend.

3.3.2 FT4233H Pins used in a Synchronous or Asynchronous Bit-Bang Interface

The FT4233H channel A, B, C or channel D can be configured as a bit-bang interface. There are two types of bit-bang modes: synchronous and asynchronous.

When configured in any bit-bang mode (synchronous or asynchronous), the pins used and the descriptions of the signals are shown in **Table 3.8**

Channel Number	Name	Type	Synchronous or Asynchronous Bit-Bang Configuration Description
A	ADBUS[7:0]	I/O	Channel A, D7 to D0 bidirectional bit-bang data
B	BDBUS[7:0]	I/O	Channel B, D7 to D0 bidirectional bit-bang data

C	CDBUS[7:0]	I/O	Channel C, D7 to D0 bidirectional bit-bang data
D	DDBUS[7:0]	I/O	Channel D, D7 to D0 bidirectional bit-bang data

Table 3.8 Channel A, B, C & D Synchronous/Asynchronous Bit-Bang Configured Pin Descriptions

For a functional description of this mode, please refer to section **Error! Reference source not found. Error! Reference source not found.**

3.3.3 FT4233H pins used in an MPSSE

The FT4233H channel A and channel B, each have a Multi-Protocol Synchronous Serial Engine (MPSSE). Each MPSSE can be independently configured to a number of industry standard serial interface protocols such as JTAG, I^2C or SPI, or it can be used to implement a proprietary bus protocol. For example, it is possible to use one of the FT4233H's channels (e.g. channel A) to connect to an SRAM configurable FPGA such as supplied by Altera or Xilinx. The FPGA device would normally be un-configured (i.e. have no defined function) at power-up. Application software on the PC could use the MPSSE to download configuration data to the FPGA over USB. This data would define the hardware function on power up. The other MPSSE channel (e.g. channel B) would be available for another serial interface function while channel C and channel D can be configured as UART or bit-bang mode. Alternatively each MPSSE can be used to control a number of GPIO pins. When configured in this mode, the pins used and the descriptions of the signals are shown in **Table 3.9**

Name	Type	MPSSE Configuration Description
TCK/SK	OUTPUT	Clock Signal Output. For example: JTAG – TCK, Test interface clock SPI – SK, Serial Clock
TDI/DO	OUTPUT	Serial Data Output. For example: JTAG – TDI, Test Data Input SPI – DO, serial data output
TDO/DI	INPUT	Serial Data Input. For example: JTAG – TDO, Test Data output SPI – DI, Serial Data Input
TMS/CS	OUTPUT	Output Signal Select. For example: JTAG – TMS, Test Mode Select SPI – CS, Serial Chip Select
GPIOL0	I/O	General Purpose input/output
GPIOL1	I/O	General Purpose input/output
GPIOL2	I/O	General Purpose input/output
GPIOL3	I/O	General Purpose input/output

Table 3.9 Channel A and Channel B MPSSE Configured Pin Descriptions

For a functional description of this mode, please refer to section **Error! Reference source not found.**.

When either Channel A or Channel B or both channels are used in MPSSE mode, Channel C and Channel D can be configured as asynchronous serial interface (RS232/422/485) or Bit-Bang mode or a combination of both.

4 Function Description

The FT4233H is a USB 2.0 High Speed (480Mb/s) to UART/MPSSE IC with USB Type-C/PD ports. It has the capability of being configured in a variety of industry standard serial interfaces.

The FT4233H has four independent configurable interfaces. Two of these interfaces can be configured as UART, bit-bang mode or JTAG, SPI, I^2C mode, using the MPSSE, with independent baud rate generators. The remaining two interfaces can be configured as UART or bit-bang.

The FT4233H has two Type-C/PD ports, with PD1 port supporting both power sink and source roles (DRP), and PD2 port works as a power sink port. Both PD ports support 5V, 9V, 15V and 20V PDO profiles, and these profiles are configurable through the external EEPROM at power-up or reset. PD1 port share the same Type-C connector with USB data, and PD2 port is power port only without USB data.

4.1 Key Features

USB Type-C/PD Controller. The FT4233H has 2 USB Type-C and PD port controllers.

USB High Speed to Quad Interface. The FT4233H is a USB 2.0 High Speed (480Mbits/s) to four independent flexible/configurable serial interfaces. This function is backward compatible to FT4232H.

Functional Integration. The FT4233H integrates a USB protocol engine which controls the physical Universal Transceiver Macrocell Interface (UTMI) and handles all aspects of the USB 2.0 High Speed interface. The FT4233H includes an integrated +1.8V Low Drop-Out (LDO) regulator and 12MHz to 480MHz PLL. It also includes 2kbytes Tx and Rx data buffers per channel. The FT4233H effectively integrates the entire USB protocol on a chip.

MPSSE. Multi-Purpose Synchronous Serial Engines (MPSSE), capable of speeds up to 30 Mbits/s, provides flexible synchronous interface configurations.

Data Transfer Rate. The FT4233H supports a data transfer rate up to 12 Mbit/s when configured as an RS232/RS422/RS485 UART interface. Please note the FT4233H does not support the baud rates of 7 Mbaud 9 Mbaud, 10 Mbaud and 11 Mbaud.

Latency Timer. This is really a feature of the driver and is used to as a timeout to flush short packets of data back to the PC. The default is 16ms, but it can be altered between 0ms and 255ms. At 0ms latency you get a packet transfer on every high speed micro frame.

4.2 Functional Block Descriptions

Type-C/PD PHY and Controller. The FT4233H has two Type-C/PD ports. Each port has Type-C/PD required Physical Layer (PHY) and controllers. PD1 port has built-in VCONN switches supporting up to 100mW VCONN power.

PD Policy Engine. The PD policy engine is a 32bit RISC processor with 8kB data RAM and 48kB ROM. It manages both PD port 1 and port 2. Default PD configurations are stored in the ROM code. PD1 port can act as power sink or source role, supporting both normal power role swap and fast role swap protocols. PD2 port acts as power sink, which can be connected to a PD charger. By using an external EEPROM, it is possible to change the PD configuration based on specific use cases, such as port 1 sink, port 1 DRP or PD charge through from port 2 to port 1. PDO voltage/current profiles can also be customised using EEPROM.

I2C Slave Interface. The application can also choose to control the PD policy by external MCU through I2C interface. In this case the built-in PD policy engine is halted. The external MCU has full control to the two PD controller registers through I2C access. An interrupt signal is also provided, so that an interrupt to an external MCU could be asserted when a PD event occurs.

GPIO block. The GPIO block provides up to 8 GPIO pins which can be used as power switch controls based on the PD policy and profiles.

Quad Multi-Purpose UART/MPSSE Controllers. The FT4233H has four independent UART/MPSSE Controllers. These blocks control the UART data or control the Bit-Bang mode if selected by the SETUP

command. The blocks used on channel A and channel B also contain a MPSSE (Multi-Protocol Synchronous Serial Engine) in each of them which can be used independently of each other and the remaining UART channels. Using this, the device can be configured under software command to have 1 MPSSE + 3 UARTS (each UART can be set to Bit Bang mode to gain extra I/O if required) or 2 MPSSE + 2 UARTS.

USB Protocol Engine and FIFO control. The USB Protocol Engine controls and manages the interface between the UTMI PHY and the FIFOs of the chip. It also handles power management and the USB protocol specification.

Dual Port FIFO TX Buffer (2Kbytes per channel). Data from the Host PC is stored in these buffers to be used by the Multi-purpose UART/FIFO controllers. This is controlled by the USB Protocol Engine and FIFO control block.

Dual Port FIFO RX Buffer (2Kbytes per channel). Data from the Multi-purpose UART/FIFO controllers is stored in these blocks to be sent back to the Host PC when requested. This is controlled by the USB Protocol Engine and FIFO control block.

RESET Generator - The integrated Reset Generator Cell provides a reliable power-on reset to the device internal circuitry at power up. The RESET# input pin allows an external device to reset the FT4233H. RESET# should be tied to VCCIO (+3.3v) if not being used.

Independent Baud Rate Generators - The Baud Rate Generators provide an x16 or an x10 clock input to the UART's from a 120MHz reference clock and consist of a 14 bit pre-scaler and 4 register bits which provide fine tuning of the baud rate (used to divide by a number plus a fraction). This determines the Baud Rate of the UART which is programmable from 183 baud to 12 million baud. The FT4233H does not support the baud rates of 7 Mbaud 9 Mbaud, 10 Mbaud and 11 Mbaud.

See FTDI application note AN232B0-5 for more details.

LDO Regulator. The +1.2V LDO regulator generates the +1.2 volts for the core and the USB transceiver cell. Its input (VREGIN) must be connected to a +3.3V external power source. It is also recommended to add an external filtering capacitor to the VREGIN. There is no direct connection from the +1.2V output (VREGOUT) and the internal functions of the FT4233H. The PCB must be routed to connect VREGOUT to the pins that require the +1.2V including VREGIN.

USB HS PHY. The Universal Transceiver Macrocell Interface (UTMI) physical interface cell. This block handles the Full speed / High Speed SERDES (serialise – de-serialise) function for the USB TX/RX data. It also provides the clocks for the rest of the chip. A 12 MHz crystal should be connected to the OSCI and OSCO pins. A 12K Ohm resistor should be connected between REF and GND on the PCB.

EEPROM Interface. EEPROM is optional. When used without an external EEPROM the FT4233H defaults to a quad USB to an asynchronous serial port device with default profiles on 2 Type-C/PD ports. Adding an external 93LC66 EEPROM allows customization of USB VID, PID, Serial Number, Product Description Strings and Power Descriptor value of the FT4233H for OEM applications, as well as PD port configurations and power profiles. Other parameters controlled by the EEPROM include Remote Wake Up, Soft Pull Down on Power-Off and I/O pin drive strength.

The EEPROM must have a 16 bit wide configuration such as a Microchip 93LC66B or equivalent capable of a 1Mbit/s clock rate at VCC = 3.0V to 3.6V. The EEPROM is programmable in-circuit over USB using a utility program called FT_PROG available from FTDI's web site (**www.ftdichip.com**). This allows a blank part to be soldered onto the PCB and programmed as part of the manufacturing and test process.

If no EEPROM is connected (or the EEPROM is blank), the FT4233H will default to serial ports. The device uses its built-in default VID (0403), PID (6011) Product Description and Power Descriptor Value. In this case, the device will not have a serial number as part of the USB descriptor.

5 Contact Information

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Web Site

http://ftdichip.com

Distributor and Sales Representatives

Please visit the Sales Network page of the FTDI Web site for the contact details of our distributor(s) and sales representative(s) in your country.

Appendix A – References

Document References

AN_113, "Interfacing FT2232H Hi-Speed Devices To I2C Bus

AN_109 – "Programming Guide for High Speed FTCI2C DLL"

AN_110 – "Programming Guide for High Speed FTCJTAG DLL

AN_111 – "Programming Guide for High Speed FTCSPI DLL

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AN135 – MPSSE Basics

AN108 - Command Processor For MPSSE and MCU Host Bus Emulation Modes

TN_104, "Guide to Debugging Customers Failed Driver Installation

TN_100 USB Vendor ID/Product ID Guidelines

TN_166 FTDI Example IC Footprints

AN2232-02, "Bit Mode Functions for the FT2232

74HC595 datasheet

FT_PROG EEPROM Programming Utility

Acronyms and Abbreviations

Terms	Description
DRP	Dual Role Power
EEPROM	Electrically Erasable Programmable Read-Only Memory
FIFO	First In First Out
FPGA	Field-Programmable Gate Array
IC	Integrated Circuit
I2C	Inter Integrated Circuit
JTAG	Joint Test Action Group
LDO	Low Drop Out
LED	Light Emitting Diode
MCU	Microcontroller Unit
MPSSE	Multi-Protocol Synchronous Serial Engine
PD	Power Delivery
PLD	Programmable Logic Device

QFN	Quad Flat No-Lead
SPI	Serial Peripheral Interface
USB	Universal Serial Bus
UART	Universal Asynchronous Receiver/Transmitter
UTMI	Universal Transceiver Macrocell Interface
VCP	Virtual COM Ports

Appendix B - List of Tables and Figures

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Appendix C - Revision History

Document Title:	FT4233H HIGH SPEED USB BRIDGE WITH TYPE-C/PD CONTROLLER Datasheet
Document Reference No.:	FT_001432
Clearance No.:	FTDI#547
Product Page:	http://www.ftdichip.com/FTProducts.htm
Document Feedback:	Send Feedback

Revision	Changes	Date
1.0	Initial Release	2018-11-05